JEDEC STANDARD

EXpanded Serial Peripheral Interface (xSPI) for Non Volatile Memory Devices, Version 1.0

JESD251C

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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EXPANDED SERIAL PERIPHERAL INTERFACE (xSPI) FOR NON VOLATILE MEMORY DEVICES

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Foreword

This standard is intended for use by SoC, ASIC, ASSP, and FPGA developers or vendors interested in incorporating a controller interface having a low signal count and high data transfer bandwidth with access to multiple sources of target devices compliant with the interface. It is also, intended for use by peripheral developers or vendors interested in providing target devices compliant with the standard, including non-volatile memories, volatile memories, graphics peripherals, networking peripherals, FPGAs, sensors, etc.

This document was prepared by the JC-42.4_3 Serial Flash task group authorized by the JC-42.4 Non-Volatile Memory subcommittee.

Introduction

This standard defines a low signal count controller-target interface for high speed byte or word serial communication with peripheral devices.

The standard defines commands for general purpose read and write of any type of peripheral device and specific commands for non-volatile memory device functions. The standard includes limited hardware and software backward compatibility with Serial Peripheral Interface (SPI) controllers widely used in the electronics industry.

Electrical DC and AC characteristics are defined for operation with a 3 V, 1.8 V, or 1.2 V power supply.

Signaling protocols are defined for command and data transfers widths of 1, or 8 bits using either Single Data Rate (SDR) or Double Data Rate (DDR) transfers at up to 200 MHz with up to 400 MT/s.

Also, defined is a Fine-pitch Ball Grid Array (FBGA) footprint with package outline options compliant with JEDEC Publication No. 95 (JEP95), MO-234.

The purpose of this standard is to define a minimum set of requirements for JEDEC standard compliance. There are a number of existing devices that may contain legacy and/or unique manufacturer's functions in addition to the minimum JEDEC requirements. Some of these functions are defined in this document as optional operations.

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eXPANDED SERIAL PERIPHERAL INTERFACE (XSPI) FOR NON VOLATILE MEMORY DEVICES

From JEDEC Board Ballot JCB-21-68, formulated under the cognizance of the JC-42.4 Subcommittee on Non-Volatile Memory Devices, item 1775.74.

1 Scope

This standard specifies the eXpanded Serial Peripheral Interface (xSPI) for Non Volatile Memory Devices, which provides high data throughput, low signal count, and limited backward compatibility with legacy Serial Peripheral Interface (SPI) devices. It is primarily for use in computing, automotive, Internet Of Things (IOT), embedded systems and mobile systems, between host processing and peripheral devices. The xSPI electrical interface can deliver up to 400 MBytes per second raw data throughput.

2 Normative Reference

The following normative documents contain provisions that through reference in this text, constitutes provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated. For undated references, the latest edition of the normative document referred to applies.

JEDEC Manual, JM7.01, *Style Manual for Standards and Other Publications of JEDEC.*

JEDEC Standard, JESD88E, *Dictionary of Terms for Solid-State Technology.*

JEDEC Standard, JESD99C, *Terms, Definitions, and Letter Symbols for Microelectronic Devices.*

JEDEC Standard, JESD100B.01, *Terms, Definitions, and Letter Symbols For Microcomputers, Microprocessors, and Memory Integrated Circuits.*

JEDEC Publication No. 95, MO-234, *Low Profile Rectangular Ball Grid Array Family, 6.00 x 8.00 x 1.20 or 1.00 mm, 24 ball package.*

JEDEC Standard, JESD8-26, *1.2 V High-Speed LVCMOS (HS_LVCMOS) Interface.*

JEDEC Standard, JESD8-31, *1.8 V High-Speed LVCMOS (HS_LVCMOS) Interface.*

JEDEC Standard, JESD8-xx, *3 V High-Speed LVCMOS (HS_LVCMOS) Interface. (In progress)*

JEDEC Standard, JESD216, *Serial Flash Discoverable Parameters (SFDP).*

JEDEC Standard, JESD252, *Serial Flash Reset Signaling Protocol.*

JEDEC Standard, JESD84-B51, *eMMC HS400 mode.*

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3 Terms and Definitions

The current version of JESD88, Dictionary of Terms for Solid-State Technology, is the governing document for terms used in this standard. The following terms and definitions are provided for ease of reference:

byte (B): (1) A binary character string operated upon as a unit and usually shorter than a computer word. (Ref. ANSI X3.172.)

NOTE A byte is usually eight bits. Within this standard, it is an 8-bit data value with the most significant bit as bit 7 and the least significant bit as bit 0.

Controller: An xSPI device that drives chip select signals to enable one other xSPI device to receive or transmit data on the interface at a given time.

Data Strobe (DS): Target to controller strobe signal to capture read data sent by the target. Target to controller signal to indicate additional initial access latency needed by the target. Controller to target signal to indicate masking of individual bytes within write data words. DS initial latency indication and write data mask behavior is used by a limited subset of xSPI commands.

Double Data Rate (DDR): Information (e.g., command, modifier, address, or data) is transferred on each edge of a related clock.

double word: A character string or binary element string that, in a given system, has twice the length of a word.

NOTE For the purpose of this document "**Dword**" is a 32-bit data value with most significant bit labeled as bit 31 and least significant bit as bit 0.

Single Data Rate (SDR): Information (e.g., command, modifier, address, or data) is transferred on one edge of a related clock.

flash EEPROM (FEEPROM): An EEPROM in which clearing can be performed only on blocks or on the entire array.

NOTE For the purpose of this document "**Flash**" is a type of block erased, multiple time programmable, nonvolatile memory.

gigabyte (GB): commonly used as a prefix to units of semiconductor storage capacity and meaning 230 [1 073 741 824] bytes

host: The computer system, test system, or other device that writes data to, and reads data from, a memory device. Within this standard, it is an xSPI controller**:** An entity or a device with the characteristics of a primary computing device that includes one or more xSPI controllers. The xSPI controller drives out all chip select (CS) signals to xSPI target devices to select one target device at a time to interact with the controller. The controller provides transfer type and address information to target devices.

HS400: High Speed DDR interface timing mode of eMMC (JESD84), with up to 400 MT/s at 200 MHz

LOW, HIGH: Binary interface states with defined assignment to a voltage level. LOW is $\leq V_{IL}$ or V_{OL}, HIGH is $\geq V_{IH}$ or V_{OH}.

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3 Terms and Definitions (cont'd)

Kilobyte (Kbyte, KB): 1024 or 2^{10} bytes.

mega (M) (as a prefix to units of semiconductor storage capacity): A multiplier equal to 1 048 576 (2^{20} or K^2, where K = 1024).

Megabyte (MB): 1,048,576 or 2^{20} bytes.

open-drain output: An open-circuit output whose internal connection is to the drain of a field effect transistor.

NOTE Within this standard, it is an output operation mode where an external resistor or current source is used to pull the output level to HIGH, and an internal transistor pulls the output level to LOW. Multiple outputs of this type from different devices may be tied together to create a wire-NOR signal.

peripheral equipment: In a data processing system, any equipment, distinct from the central processing unit, that may provide the system with outside communication or additional facilities. (Ref. ANSI X3.172.)

NOTE For the purpose of this document "**peripheral**" refers to an xSPI target, see definition.

Power On Reset (POR): A hardware reset process that leaves the device in a defined state, triggered by the rise of power supply voltage levels from near ground to the operating range level.

push-pull output: Two open-circuit outputs operating in complementary fashion so that as the resistance of one increases, the resistance of the other decreases. Within this standard, an output operation mode where a complementary pair of transistors is used to alternately push the interface level to HIGH or pull it to LOW.

quad word: A character string or binary element string that, in a given system, has four times the length of a word. Within this standard: a 64-bit data value with most significant bit labeled as bit 63 and least significant bit as 0.

Target: An xSPI device that receives a chip select signal to enable receive or transmit of data on the interface at a given time.

word: A character string or a binary element string that it is convenient to consider as an entity. (Adapted from ANSI X3.172.)

NOTE For memories, it is common practice to use the term "word" generically for any number of bits that occupy a single address location. Within this standard: a 16-bit data value with most significant bit labeled as bit 15 and least significant bit as bit 0.

xSPI target: An entity or a device with the characteristics of peripheral equipment that is selected by an xSPI controller.

NOTE The xSPI target is made active by its chip select (CS#) input to interact with the controller. The target receives transfer type and address information in order to identify which data to receive from or transmit to the xSPI controller.

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3.1 Acronyms

DDR	Double Data Rate. Data is transferred on each edge of a related clock.
GB	Gigabyte: 1,073,741,824 or 2^{30} bytes.
I/O or IO	Input or Output – A signal port that may receive or drive voltage levels to communicate with other devices.
KB	Kilobyte: 1024 or 2^{10} bytes.
MB	Megabyte: 1,048,576 or 2^{20} bytes
MB/s	Megabytes per second
MSb, LSb	Most Significant Bit or Least Significant Bit
MT/s	Mega Transfers per second
NVM	Non-Volatile Memory
UI	Unit Interval; It is one bit nominal time. For example, UI=5 ns at 200 MHz SDR, UI = 2.5 ns for 200 MHz DDR.
xSPI	eXtended Serial Peripheral Interface

3.2 Conventions

This standard follows some conventions used in other JEDEC documents.

A binary number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 and 1 immediately followed by a lower-case b (e.g., 0101b). Spaces may be included in binary number representations to increase readability or delineate field boundaries (e.g., 0 0101 1010b).

A hexadecimal number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 through 9 and/or the upper-case English letters A through F immediately followed by a lower-case h (e.g., FA23h). Spaces may be included in hexadecimal number representations to increase readability or delineate field boundaries (e.g., B FD8C FA23h).

A decimal number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 through 9 not immediately followed by a lower-case b or lower-case h (e.g., 25).

A range of numeric values is represented in this standard in the form "a to z", where a is the first value included in the range, all values between a and z are included in the range, and z is the last value included in the range (e.g., the representation "0h to 3h" includes the values 0h, 1h, 2h, and 3h).
Other conventions used in this document:

Signals that are considered active when LOW have signal names that end with the hash / pound special character (i.e., have a suffix of #).

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3.3 Keywords

Several keywords are used to differentiate levels of requirements and options, as follow:

Can - A keyword used for statements of possibility and capability, whether material, physical, or causal (can equals is able to).

Expected - A keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

Ignored - A keyword that describes bits, bytes, or fields whose values are not checked by the recipient.

Mandatory - A keyword that indicates items required to be implemented as defined by this standard.

May - A keyword that indicates a course of action permissible within the limits of the standard (may equals is permitted).

Must - The use of the word must is deprecated and shall not be used when stating mandatory requirements; must is used only to describe unavoidable situations.

Obsolete - A keyword indicating that an item was defined in prior standards but has been removed from this standard.

Optional - A keyword that describes features which are not required to be implemented by this standard. However, if any optional feature defined by the standard is implemented, it shall be implemented as defined by the standard.

Preferred – A keyword used to identify a feature option which is the preferred option to implement for compliance with anticipated future revisions of this standard.

Reserved - A keyword used to describe objects—bits, bytes, and fields—or the code values assigned to these objects in cases where either the object or the code value is set aside for future standardization.

Usage and interpretation may be specified by future extensions to this or other standards. A reserved object shall be zeroed or, upon development of a future standard, set to a value specified by such a standard. The recipient of a reserved object shall not check its value. The recipient of a defined object shall check its value and reject reserved code values.

Shall - A keyword that indicates a mandatory requirement strictly to be followed in order to conform to the standard and from which no deviation is permitted (“shall” equals “is required to”). Designers are required to implement all such mandatory requirements to assure interoperability with other products conforming to this standard.

Should - A keyword used to indicate that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited (“should” equals “is recommended that”).

Will - The use of the word will is deprecated and shall not be used when stating mandatory requirements; will is only used in statements of fact.

3.4 Abbreviations

etc.: And so forth (Latin: et cetera)

e.g.: For example (Latin: exempli gratia)

i.e.: That is (Latin: id est)

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4 Key Features

The following is a summary of the eXtended Serial Peripheral Interface (xSPI) features:

4.1 General Features

- Speed grades with data transfer rates up to
  - 400 MT/s (200 MHz Clock)
  - 333 MT/s (167 MHz Clock)
  - 266 MT/s (133 MHz Clock)
  - 200 MT/s (100 MHz Clock)

4.2 Topology

  - Single controller, multiple targets, per interface port
    - One chip select per target

4.3 Interface Features

- Input/Output Power Supplies Options:
  - 1.2 V, 1.8 V, or 3 V

- Signal Count Options:
  - Eleven-signal target interface (Clock, CS#, 8-bit Data bus, Data Strobe)
  - Twelve-signal target interface (Differential Clock, CS#, 8-bit Data bus, Data Strobe)
  - Interface may operate in 1S-1S-1S IO mode without data strobe at ≤ 50 MHz SDR

- IO Protocol Modes:
  - Transaction phases = Command-Modifier-Data
  - Transfer bit width options in each phase = W = 1, or 8
  - Data rate options in each phase = R = S for SDR or D for DDR
  - 1S-1S-1S (24 bit addressing) for power-up and configuration
  - 8D-8D-8D (32 bit addressing in Profile 1.0 or 45 bit addressing in profile 2.0)

- Target Reset Options:
  - Power-on Reset (POR) -- mandatory
  - In-band Reset -- preferred
  - Separate Reset Signal -- optional

- Power Management Option
  - Deep Power Down (DPD) enter and exit commands

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5 xSPI Overview

5.1 xSPI Performance Enhancements

Serial interface performance can be enhanced by increasing the basic clock rate, adding source synchronous clocking, using Double Data Rate (DDR), or by adding parallel data (IO) lines. xSPI allows all four methods.

Higher clock rates with accurate information transfer are possible by using a separate clock signal for each direction of information transfer. This is known as source synchronous clocking; providing a timing reference (clock / strobe) from the source of information, with minimum skew relative to the related information (data). This enables accurate timing of information capture at the destination device as the period of valid information decreases at higher clock rates.

DDR can be used to double performance by relating information transfers to both rising and falling edges of the timing reference.

Up to 8 parallel data (IO) lines are used in xSPI to further increase system performance by transferring more parallel bits in each clock cycle.

5.2 xSPI Topology and Signal Descriptions

xSPI has a single controller, multiple target bus topology with source synchronous clocking.

Each target device is selected by a separate LOW active Chip Select (CS#) signal from the controller device.

A clock (CK) signal from the controller to all target devices provides a timing reference for interface operations. The clock is the timing reference for information transfer on the IO signals from the controller to the selected target. The clock is also a timing reference for interface operations within the controller and target interface logic, such as the counting of access latency time. The clock may optionally be provided by the controller as a differential clock using two signals (CK and CK#). The remaining text and block diagrams in this standard may only describe one clock (CK) signal for simplicity but, where ever CK is described or illustrated, a differential pair of CK, CK# may be used. Some xSPI compliant target devices require a differential clock. A differential clock reduces clock duty cycle distortion and effectively doubles the clock slew rate, providing improved timing margins for target devices using a differential clock.

The IO signals provide a bidirectional, variable width path, for information transfer between the controller and selected target. Different targets on the same bus may use a different IO width for information transfer.

The Data Strobe (DS) signal provides a timing reference for information transfer on the IO signals from the target to the controller. DS is an output signal from the xSPI target device that is aligned with the edges of output data and is used by the controller interface to optimize high frequency read data capture. DS may optionally be used as a signal from the target to the controller, to indicate the duration of initial access latency or, as a signal from the controller to the target, to indicate write data masking.

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5.2 xSPI Topology and Signal Descriptions (cont'd)

Controller and target devices may have separate power supplies and ground references for internal (core) logic functions versus the xSPI interface receiver inputs and output drivers. The ability to separate the core and IO power supplies may help to reduce IO noise injection into the core power supply. However, devices are not required to separate their core and IO power supplies. These power supplies may be tied together in parallel at the device terminals. The core power supply is labeled V_{DD} and the interface power supply is labeled $V_{DD}Q$. The core ground reference is labeled V_{SS} and the interface ground reference is labeled $V_{SS}Q$.

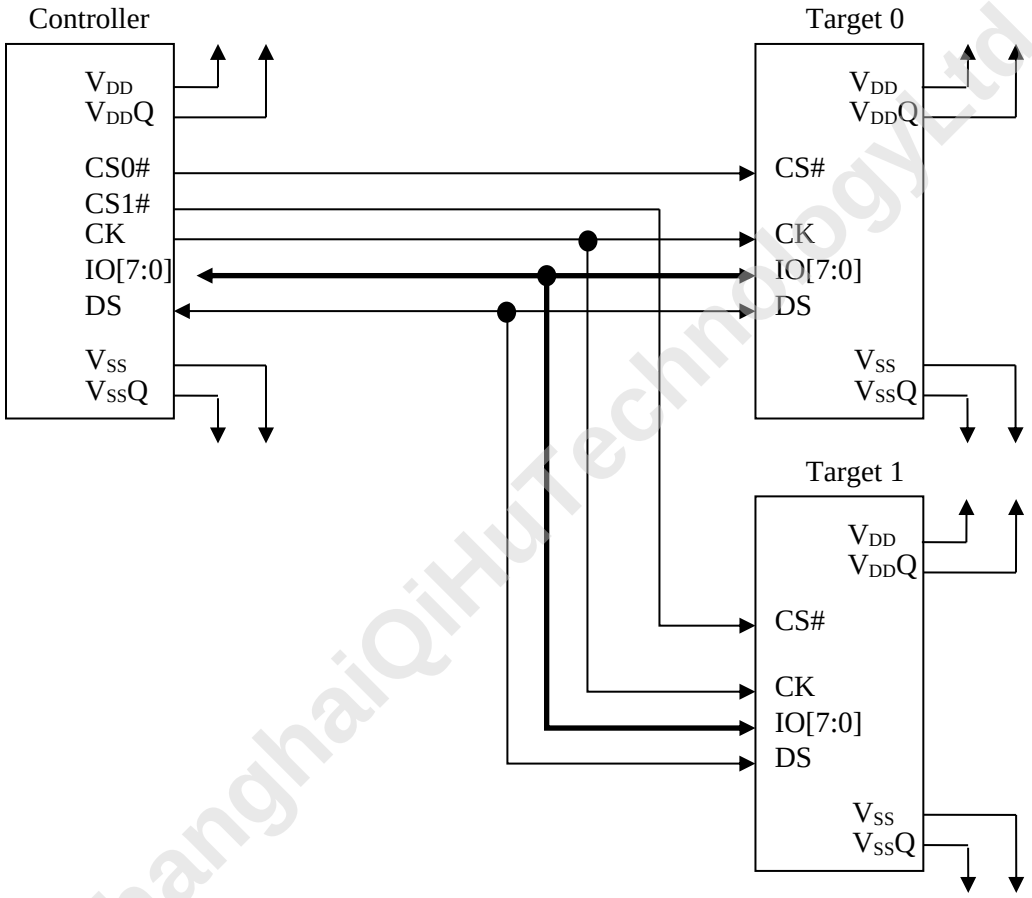

Figure 1 — xSPI System Topology

5.3 xSPI Protocol Modes

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5.4 xSPI Signal Protocols

During the time that CS# is active (LOW) the clock signal (CK) is toggled while command information is first transferred on the data (IO) signals from the controller to the target. The clock continues to toggle during any period required for information access in the target. The clock continues to toggle during the transfer of read data from the target to the controller or write data from the controller to the target. When the controller has transferred the desired amount of data, the controller drives the CS# inactive (HIGH). The period during which CS# is active is called a transaction on the bus.

While CS# is inactive, the CK is not required to toggle. CK may stop toggling when LOW as a means of lowering power consumption or inserting delay within a transaction for flow control by the controller. CK must always complete at least one rising edge and one falling edge before stopping at LOW. This requirement for a minimum of one rising and falling edge in turn requires that DDR transfers always occur in two transfer increments, e.g., two bytes (word) for 8-bit wide transfers. SDR transfers must occur in one byte increments. Some target devices may have limitations on the maximum time that CK may stop (remain LOW) or, on the maximum time CK may be HIGH (i.e., a minimum clock frequency during a transaction); these are target device specific system design consideration.

There are up to four phases of activity within each transaction:

- Command transfer from controller to target
- Command Modifier transfer from controller to target
- Initial Access Latency (also used for IO signal direction turn around in a read transaction)
- Data transfer (target to controller in a read transaction or controller to target in a write transaction)

The command transfer occurs at the beginning of every transaction. The command modifier, initial access latency, and data transfer phases are optional and their presence depends on the protocol mode or command transferred.
The number of parallel IO signals used during the command modifier and data phases depends on the current protocol mode or command transferred. The initial access latency phase does not use the IO signals for information transfer. The protocol mode options are described by the data rate and the IO width (number of IO signals) used during the command, command modifier, and data phases in the following format:

WR-WR-WR where:

- The first WR is the command bit width and rate
- The second WR is the command modifier bit width and rate
- The third WR is the data bit width and rate

The bit width value may be 1, or 8. R has a value of S for SDR, or D for DDR. SDR has the same transfer value during the rising and falling edge of a clock cycle. DDR may have different transfer values during the rising and falling edges of each clock.

Examples:

- 1S-1S-1S means that the command is 1-bit wide SDR, the command modifier is 1-bit wide SDR, and the data is one bit wide SDR.
- 8D-8D-8D means that the command, command modifier, and data transfers are always 8 bits wide DDR.

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5.4 xSPI Signal Protocols (cont'd)

Protocol Modes defined for the xSPI interface:

- 1S-1S-1S
  - One IO signal used during command transfer, command modifier transfer, and data transfer. All phases are SDR.
- 8D-8D-8D
  - Eight IO signals used during command transfer, command modifier transfer, and data transfer. All phases are DDR.

A target device must implement both of the above protocol modes.

The 1S-1S-1S mode is the preferred default protocol following Power-On-Reset (POR) but, target devices may be configured to reset into the Octal mode. Target devices may implement other modes of operation. The supported modes are indicated in the SFDP.

For example, 8D-8D-8D mode can be made the default mode if so desired. The controller must determine the default protocol mode of each target after POR. This may be done through prior knowledge of the system design. The controller may later reconfigure a target to use other target supported modes. In some devices switching between modes is done through issuing a command or a series of commands while in other devices that change is done through a modification of bits in control registers. The modes supported by a target and the method for switching between modes are indicated in the SFDP.

A protocol mode phase using single bit transfer uses IO[0] to transfer information from controller to target and IO[1] to transfer information from target to controller. On each IO, information is placed on the IO line in Most Significant bit (MSb) to Least Significant bit (LSb) order within each byte. Sequential command modifier bytes are transferred in highest order to lowest order sequence. Sequential data bytes are transferred in lowest address to highest address order.

Table 1 — 1S-1S-1S Bit Positions for 4 (and 3) Byte Addressing

IO	Command Bits	Command Modifier Bits (Address)	Latency	Data Byte 0	Data Byte 1
0	7, 6, 5, 4, 3, 2, 1, 0	31 (23), 30 (22), … 1, 0	X …	X …	X …
1	X …	X …	X …	7, 6, 5, 4, 3, 2, 1, 0	7, 6, 5, 4, 3, 2, 1, 0
2	X …	X …	X …	X …	X …
3	X …	X …	X …	X …	X …
4	X …	X …	X …	X …	X …
5	X …	X …	X …	X …	X …
6	X …	X …	X …	X …	X …
7	X …	X …	X …	X …	X …

See 6.9.5, Transaction Formats by Protocol Mode for waveform examples.

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5.4 xSPI Signal Protocols (cont'd)

A protocol mode phase using eight IO signals uses IO[7:0]. The LSb of each byte is placed on IO[0] with each higher order bit on the successively higher numbered IO signals. Sequential command modifier bytes are transferred in highest order to lowest order sequence. Sequential data bytes in SDR are transferred in lowest address to highest address order. Sequential data bytes in DDR are transferred only in byte pairs (words) where the byte order depends on the order in which the bytes are written or programmed in that protocol mode. Sequential data bytes are transferred in lowest address to highest address order.

Table 2 — 8D-8D-8D Bit Positions

IO	Command Bits	Command Modifier Bits (Command Ext. and Address)					Latency	Data Word 0		Data Word 1	
0	0	0	24	16	…	0	X …	0	0	0	0
1	1	1	25	17	…	1	X …	1	1	1	1
2	2	2	26	18	…	2	X …	2	2	2	2
3	3	3	27	19	…	3	X …	3	3	3	3
4	4	4	28	20	…	4	X …	4	4	4	4
5	5	5	29	21	…	5	X …	5	5	5	5
6	6	6	30	22	…	6	X …	6	6	6	6
7	7	7	31	23	…	7	X …	7	7	7	7

IO signals not in use in a particular phase are undefined may or may not be driven by the controller or target device; i.e., these signals may be in a high impedance state (floating and indicated by X in the bit position tables). In single bit transfers the IO[7:2] signals may be high impedance.

During the period of data transfer in a read transaction, the Data Strobe (DS) signal is driven by the target and transitions edge aligned with the IO signal data transitions. DS is used as an additional output signal with the same timing characteristics as other data outputs but with the guarantee of transitioning with every data bit transferred. The DS signal transitions can be received and internally phase shifted by the controller to be used as an internal read data clock to capture each data bit transferred.

DS transitions may have deterministic or variable timing with reference to CK. Some target devices may be deterministic and delay the toggling of DS for a fixed number of cycles during the initial access latency period then always follow CK transitions during the remainder of a transaction. Some target devices may have variable DS timing by delaying the toggling of DS for a variable number of cycles during the initial access latency phase and then may delay toggling during some following data transfer phase CK cycles – as a means of flow control on target to controller information transfers. However, like CK, DS must always delay (stop) when LOW and always have one rising and falling edge before stopping.

The deterministic or variable DS behavior is target device specific. The controller may treat a delay of DS toggling for more than a number of CK cycles as a transaction error and end the transaction by taking CS# HIGH. The variable or deterministic DS behavior and the number of cycles indicating an error are indicated in the SFDP.

Some commands define other functions for DS during the command and command modifier phase or during write data transfers. These additional functions are described in the command descriptions.

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5.5 Legacy SPI Compatibility

xSPI target devices support the 1S-1S-1S protocol for limited backward compatibility with the legacy single IO Serial Peripheral Interface (SPI) protocol. The 1S-1S-1S mode supports a limited subset of SPI protocol commands, to enable basic target device identification in the same protocol used by legacy SPI target devices. This backward compatibility can simplify the POR and configuration process for systems that may use legacy SPI targets on the xSPI interface signals. Once each target device is identified, it is expected that the protocol will be switched to 8D-8D-8D.

6 xSPI Transaction Descriptions

6.1 Target Selection

Each transaction starts with CS# for a particular target device going from HIGH to LOW. Each transaction ends when that CS# returns from LOW to HIGH. While the CS# is HIGH, the target ignores all other xSPI signals. While CS# is LOW, the CK signal edges cause the transfer of information on the IO signals. CS# must transition from HIGH to LOW or LOW to HIGH while CK is LOW. Thus, CK is LOW when idle or stopped, and is equivalent to the legacy SPI Mode 0 with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0. This is the only legacy SPI clock mode supported in xSPI.

6.2 Clock, DS, and Information Transfer

The clock may be a free running (always toggling) signal but is recommended to only toggle while CS# is LOW to minimize power consumption. CK signal edges cause the transfer of information on the IO signals. If the differential clock option is used, the crossing point of CK and CK# causes the transfer of information on the IO signals.

NOTE A free running clock will meet the timing in this standard only at relatively low frequencies. For high frequency operation, clock should be gated.

During information transfer from controller to target, the IO signals are driven to a valid HIGH or LOW state for at least a set-up time (t_{SU}) before a CK edge and are held valid for at least a hold time (t_{IH}) after the CK edge – the CK edge is within the valid IO (data) window. This occurs during the command, command modifier, and write data phases of a transaction.

During an initial access latency phase no information is transferred but CK toggles to act as a timing reference to target device interface logic so that it progresses through the initial access process for data. Legacy SPI protocols sometimes referred to this phase as Dummy cycles.

During information transfer from target to controller; i.e., a read data transfer phase, CK continues to toggle so that the target interface progresses through the read data transfer process. However, CK is not the timing reference for when read data is valid. During a read data phase, DS toggles edge aligned with the IO signals to serve as the read data timing reference. However, for backward compatibility with legacy SPI targets, in the 1S-1S-1S mode, the controller may use CK as the timing reference for read data. This legacy SPI compatible method of clocking read data may be restricted to lower frequency operation depending on the controller and target output driver characteristics. The frequency expectation for commands operating without DS is indicated in the SFDP.

Some commands use DS during the command and command modifier phases to indicate an extension of the initial latency phase. Some commands use DS during a write data phase as a data mask to control byte writes.

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6.3 Command Phase

An eight bit command is always the first information transferred in a transaction. The first transfer of command bits happens on the first rising edge of CK after CS# is LOW. In an SDR protocol, any additional command bit transfers occur on the following rising CK edges until the command is completely transferred. In 1S-1S-1S protocol mode this requires 8 rising CK edges. In 8D-8D-8D protocol mode the command is transferred by the first rising edge of CK.

The command transferred determines the format of any remaining transfers during the transaction.

The xSPI protocol uses a subset of the same 8-bit command codes as in the de-facto legacy SPI protocol. To simplify the design of both the controller and target device interfaces, the commands supported vary depending on the protocol mode in use. The xSPI protocol also adds some new command codes not found in legacy SPI protocols.

NOTE Some xSPI devices have a mode in which the command phase is not required. While in this mode, commonly called XiP Mode, the controller skips sending the command and the target device implicitly performs the command that was executed in the previous transaction. While in a current transaction, the controller may indicate that the next transaction will also be in XiP Mode by sending a pre-defined data value during the initial latency phase.

6.4 Command Modifier Phase

Some commands have no following information transfer. These are single byte commands that need no additional information. The transaction ends with CS# returning HIGH after such a command is transferred.

Some commands are followed by an additional byte that serves to further define or confirm the command behavior. In the command summary tables, the Command Extension column indicates:

- **NA** – Not Applicable, for commands that do not have a command extension byte. In this standard, NA is only used in 1S-1S-1S mode.
- **RI** – Repeat or Invert, for commands that either transfer the command again or transfer a bitwise inverted copy of the command as the command extension. It is target specific as to whether a repeated or inverted command is expected. The expectation is indicated in the SFDP. In this standard, RI is only used in profile 1.0 of 8D-8D-8D mode. Note that in this mode the host device must send either a repeated or inverted command while the target device is not required to read both.
- **Hex value** – for commands that use the command extension byte to further define the command function, the specific hexadecimal value of the command extension byte is shown. In this standard, Hex is only used in profile 2.0 of 8D-8D-8D mode.

Some commands or a command extension byte are followed by multiple bytes of additional command modifier that is generally used as an address within a memory array. The number of additional modifier bytes may be defined by the command or depend on a modifier (address) length configuration. The number of additional modifier bytes is shown in the additional modifier column of the command summary tables. A zero indicates that no additional modifier bytes are provided.

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6.5 Initial Access Latency Phase

Some commands have no following information transfer. These commands need no additional information transfer after the command modifier phase and therefore no latency phase. The transaction ends with CS# returning HIGH after such a command or command modifier is transferred.

Some commands do not need a latency period before transferring data. Some read commands require data transfer on the cycle following the command modifier phase. Generally, target devices will restrict the use of these commands to lower operating frequencies. Some write commands requires data transfer on the cycle following the command modifier phase.

In the command summary tables a zero (0) in the Initial Access Latency column indicates the command is deterministic and has no initial access latency phase. A non-zero value indicates a deterministic initial access latency. A value of zero or a number plus (0+, 1+, …) indicates the command has a minimum initial latency that may vary based on a configuration setting or other conditions present during the transaction. Whether the command has deterministic, configurable, or variable latency that requires monitoring when DS transitions is indicated in the SFDP.

6.6 Data Phase

Some commands have no following information transfer. These commands need no additional information transfer after the command modifier phase and therefore have no data phase. The transaction ends with CS# returning HIGH after such a command or command modifier is transferred.
In the command summary tables this is indicated by a zero (0) in the data bytes column.

Other commands may transfer one data byte and repeat the data byte if the transaction is continued. This is indicated as a one (1) in the data bytes column.

Other commands may transfer one or more sequential data bytes and is indicated as a one plus (1+) in the data bytes column. Other commands may always transfer an even number of sequential data bytes (always transferring two byte words) and is indicated as a two plus (2+) in the data bytes column.

6.7 Required versus Optional Commands

Some commands that are required, if a protocol mode and command type subset is supported, are listed in the command summary Table 3 Commands used in 1S-1S-1S protocol mode (required commands) and Table 4 Profile 1.0 commands used in 8D-8D-8D protocol mode (required commands) Optional commands are listed in command summary Table 5 Profile 1.0 commands used in 8D-8D-8D protocol mode (optional commands).

Many commands are optional. The commands that are supported by a target device must be indicated in the SFDP.

However, in 8D-8D-8D protocol mode there are two command profiles that although optional as a profile, some commands from one, the other or, both of the command profiles must be supported. These command profiles are:

- Profile 1.0
- Profile 2.0

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6.7 Required versus Optional Commands (cont'd)

Profile 1.0 commands directly affect information in memory target devices. The commands may read from a memory array, write to registers, program non-volatile memory, erase non-volatile memory, etc.

Transport commands are not specific to memory devices. These commands move data into (write) or out of (read) a target xSPI device in a general purpose way. The commands read or write to either a memory address space or a register address space. The commands also specify whether the read or write transfers data in a linear or wrapped sequence. The meaning of the data transferred is target device specific. The target device accessed by these commands may be a volatile or non-volatile memory or some type of peripheral such as a graphics display, or network adapter, or some other function implemented in a Field Programmable Gate Array (FPGA).

If a command is required when Profile 1.0 is supported, it is indicated with 1 in the Req. column. If a command is required when Profile 2.0 is supported, it is indicated with 1 in the Req. column.

It is compliant with the xSPI standard to implement the required commands from either the required Profile 1.0 commands, or the required Profile 2.0 commands or, the required commands from both of these profiles.

6.8 Maximum Frequency

Some commands, if supported, are only required to operate at or below a maximum frequency. If a maximum frequency is defined for a command it is shown in the maximum frequency column of the command summary tables.

6.9 Command Summary Tables

The main characteristics of commands for each protocol mode are summarized in the following tables. Details of each command implementation are in the Command Description clauses.

6.9.1 1S-1S-1S Mode

Table 3 shows the required commands in the 1S-1S-1S protocol mode. It is expected that this mode will be used only for identification and configuration of the target device. As soon as the device is identified and configured, it is expected that the target device will be switched to a higher data rate protocol mode. See 6.10.2.21 Enter Another Protocol Mode for more information. Note that each command uses one of the Transaction Formats described in 6.9.5 Transaction Formats by Protocol Mode.

Table 3 — Commands Used in 1S-1S-1S Protocol Mode (Required Commands)

Command Function	Command Code (Hex)	Command Extension (Hex)	Additional Modifier Bytes	Initial Latency (CK Cycles)	Data Bytes	Req.	Transaction Format	Req. Freq. (MHz)
Read SFDP	5A	NA	3	8	1+	1	0.E	50+
Read Zero Latency	03	NA	3	0	1+	1	0.C	50+

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6.9.2 8D-8D-8D Profile 1.0

Commands are grouped into two Categories:

6.1 Category 1: Non-WREN Enabled Commands require a single CS# cycle

6.2 Category 2: WREN Enabled Commands must be prefixed by one additional CS# cycle for a write enable (WREN) command

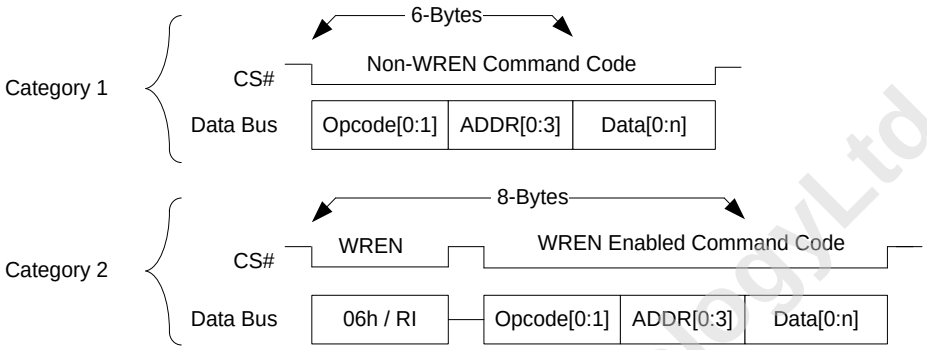

Figure 2 — Command Categories

Table 4 — Profile 1.0 Commands Used in 8D-8D-8D Protocol Mode (Required Commands)

Command Function	Command Code (Hex)	Category	Command Extension (Hex)	Additional Modifier Bytes	Initial Latency (CK Cycles)	Data Bytes	Transaction Format	Req. Max. Freq. (MHz)
Read Fast	0B / EE / SFDP	1	RI	4	1+	2+	1.B	
Write Enable (WREN)	06	1	RI	0	0	0	1.A	
Write Disable	04	1	RI	0	0	0	1.A	
Program	02 / 12 / SFDP	2	RI	4	0	2+	1.D	
Erase 64+Kbytes	D8 / DC / SFDP	2	RI	4	0	0	1.C	
Program / Erase Suspend	B0 / 75 / SFDP	1	RI	0	0	0	1.A	
Program / Erase Resume	30 / 7A / D0 / SFDP	1	RI	0	0	0	1.A	
Read Status Register	05	1	RI	0 / 4 / SFDP	4 / 8 / SFDP	1	1.B	

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6.9.2 8D-8D-8D Profile 1.0 (cont'd)

Table 5 — Profile 1.0 Commands Used in 8D-8D-8D Protocol Mode (Optional Commands)

Command Function	Command Code (Hex)	Category	Command Extension (Hex)	Additional Modifier Bytes	Initial Latency (CK cycles)	Data Bytes	Transaction Format	Req. Max. Freq. (MHz)
Read SFDP 8D-8D-8D	5A	1	RI	3 / 4	8 / 20	2+	1.B	50+
Read Fast Wrapped	0C / SFDP	1	RI	4	1+	2+	1.B	
Setup Read Wrap	C0	1	RI	4	0	2+	1.D	
Erase 4Kbytes	20 / 21 / SFDP	2	RI	4	0	0	1.C	
Erase 32Kbytes	52 / 53 / SFDP	2	RI	4	0	0	1.C	
Erase Chip	C7	2	RI	0	0	0	1.A	
Read Configuration Register	15	1	RI	4	4	1	1.B	
Read Flag Status Register	70	1	RI	0	8	1	1.A	
Read Register	65	1	RI	1/ 4 / SFDP	1+	1+	1.B	
Read Volatile Register	85 / 71 SFDP	1	RI	4	4 / 8 / SFDP	1	1.B	
Read NV Register	B5 / 15 / 65 / SFDP	1	RI	4	4 / 8 / SFDP	1	1.B	
Write Status-Configuration Register	01	2	RI	0 / 4 / SFDP	0	1+	1.D	
Clear Flag Status Register	50	1	RI	0	0	0	1.A	
Write Register	71 / SFDP	2	RI	1/ 4 / SFDP	0	1 / 2	1.D	
Write Volatile Register	81 / 72 / 71 / SFDP	2	RI	4	0	1	1.D	
Write NV Register	B1 / 01 / 71 / SFDP	2	RI	4	0	1	1.D	
Enter Deep Power Down	B9	1	RI	0	0	0	1.A	
Exit Deep Power Down	AB	1	RI	0	0	0	1.A	
Soft Reset	F0	1	RI	1	0	0	1.B	
Reset Enable	66	1	RI	0	0	0	1.A	
Soft Reset and Enter default protocol mode	99	1	RI	0	0	0	1.A	
Enter default protocol mode	FF	1	RI	0	0	0	1.A	

NOTE 1 New device designs should assign Command Codes from the above tables for commands that are specified in the table rather than pick other codes

NOTE 2 It is recommended that new device designs should only pick Command Codes that are not mentioned in the above tables for new commands.

NOTE 3 The size of block erased by the Erase 64+Kbytes and Erase 64+Kbytes4 command is indicated in the SFDP.

NOTE 4 Some commands have multiple recommended code value options that are device specific. New device designs should pick one of the recommended code values. The device supported command codes are indicated in the SFDP. This is indicated in the table by listing SFDP as one of the command code options.

NOTE 5 Some commands have multiple recommended command modifier length options that are device or device configuration specific. New device designs should pick one of the recommended command modifier lengths. The target device supported command modifier length options and any configuration methods are indicated in the SFDP.

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6.9.3 8D-8D-8D Profile 2.0

Instructions are categorized into four sets described as follows:

1. Instruction opcodes under Non-WREN (1 and 2) Enabled Command Code are single CS# cycle - Category 3.
2. Instruction opcodes under WREN (1 and 2) Enabled Command Code require two additional CS# cycles for write enables (1 and 2) – Category 4.
3. Instruction opcodes under Command Extension Code are additional CS# cycles to instruction cycles in category 2 – Category 5.
4. Instruction opcodes under Status Register Enabled Command Code require one additional CS# cycles for Status Register enable – Category 6.

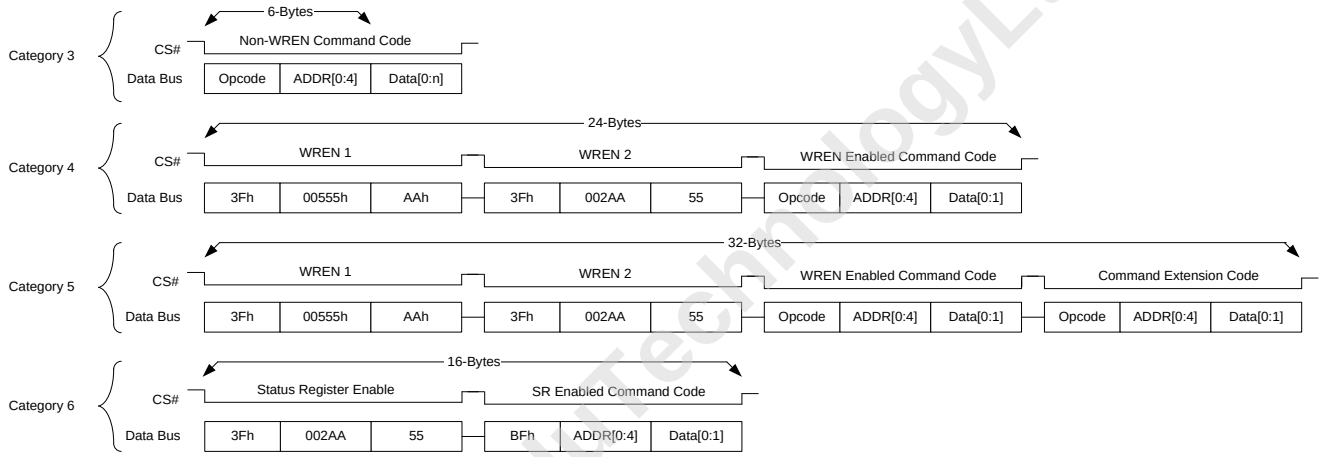

Figure 3 — Instruction Categories

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6.9.3 8D-8D-8D Profile 2.0 (cont'd)

Table 6 — Profile 2.0 Commands Used in 8D-8D-8D Protocol Mode

Command Function	Command Code (Hex)	Category	Additional Command Modifier Bytes	Initial Latency (CK Cycles)	Data Bytes	Command Extension Required	Transaction Format	Req. Max. Freq. (MHz)
Read Register Wrapped	DF	3	5	1+	2+	0	2.A	
Read Register Linear	FF	3	5	1+	2+	0	2.A	
Read Memory Wrapped	9F	3	5	1+	2+	0	2.A	
Read Memory Linear	BF	3	5	1+	2+	0	2.A	
Write Register Wrapped	5F	3	5	0+	2+	0	2.B	
Write Register Linear	7F	3	5	0+	2+	0	2.B	
Write Memory Wrapped	1F	3	5	0+	2+	0	2.B	
Write Memory Linear	3F	3	5	0+	2+	0	2.B	
Write Enable 1 (WREN1)	3F	3	5 "00555h"	0+	2 "00AAh"	0	2.B	
Write Enable 2 (WREN2)	3F	3	5 "002AAh"	0+	2 "0055h"	0	2.B	
Status Register Enable	3F	3	5 "00555h"	1+	2 "0070h"	0	2.B	
Status Register Read	BF	6	5	1+	2	0	2.A	
Status Register Clear	3F	3	5 "00555h"	0	2 "0071h"	0	2.B	
Enter Deep Power Down Mode	3F	4	5	0	2 "00B9h"	0	2.B	
Configuration Register Load (Volatile)	3F	4	5 "00555h"	0	2 "0038h"	1	2.B	
Configuration register Load (Volatile) - Extension	3F	5	5	0	2	0	2.B	
Configuration Register Read (Volatile)	3F	4	5 "00555h"	0	2 "00C7h"	1	2.B	
Configuration Register Read (Volatile) – Extension	BF	5	5	0	2	0	2.A	
Configuration Register Program (Non-Volatile)	3F	4	5 "00555h"	0	2 "0039h"	1	2.B	
Configuration Register Program (Non-Volatile) - Extension	3F	5	5	0	2	0	2.B	
Configuration Register Erase (Non-Volatile)	3F	4	5 "00555h"	0	2 "00C8h"	0	2.B	
Configuration Register Read (Non-Volatile)	3F	4	5 "00555h"	0	2 "00C6h"	1	2.B	
Configuration Register Read (Non-Volatile) – Extension	BF	5	5	0	2	0	2.A	
Word Program	3F	4	5 "00555h"	0	2 "00A0h"	1	2.B	
Word Program – Extension	3F	5	5	0	2	0	2.B	
Write to Buffer – 256B	3F	4	5 "SA[1]"	0	2 "0025h"	1	2.B	
Write to Buffer – 256B – Extension 1	3F	5	5	0	2 "WC[2]"	1	2.B	
Write to Buffer – 256B – Extension 2	3F	5	5	0	2	1+	2.B	

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Table 6 — Profile 2.0 Commands Used in 8D-8D-8D Protocol Mode (cont'd)

Command Function	Command Code (Hex)	Category	Additional Command Modifier Bytes	Initial Latency (CK Cycles)	Data Bytes	Command Extension Required	Transaction Format	Req. Max. Freq. (MHz)
Program Write to Buffer (Confirm)	3F	3	5 "SA[1]"	0+	2 "0029"	0	2.B	
Sector Erase	3F	4	5 "00555h"	0	2 "0080h"	1	2.B	
Sector Erase – Extension 1	3F	5	5	0	2 "00AAh"	1	2.B	
Sector Erase – Extension 2	3F	5	5	0	2 "0055h"	1	2.B	
Sector Erase – Extension 3	3F	5	5 "SA[1]"	0	2 "0030h"	0	2.B	
Chip Erase	3F	4	5 "00555h"	0	2 "0080h"	0	2.B	
Chip Erase – Extension 1	3F	5	5	0	2 "00AAh"	1	2.B	
Chip Erase – Extension 2	3F	5	5	0	2 "0055h"	1	2.B	
Chip Erase – Extension 3	3F	5	5 "00555h"	0	2 "0010h"	0	2.B	
Erase Suspend	3F	3	5	0+	2 "00B0"	0	2.B	
Erase Resume	3F	3	5	0+	2 "0030"	0	2.B	
Program Suspend	3F	3	5	0	2 "0051h"	0	2.B	
Program Resume	3F	3	5	0	2 "0050h"	0	2.B	
Read SFDP	3F	4	5 "00555h"	0	2 "0090h"	1	2.B	
Read SFDP – Extension	BF	5	5	0	2+	0	2.A	
Enter Default Protocol Mode	3F	4	5 "00555h"	0	2 "00F5h"	0	2.B	

6.9.4 Command Summary Notes

- The SFDP indicates which of the optional commands are implemented.
- SFDP read commands must be 4-byte aligned (Profile 1.0).
- The Read and Write Register commands can be used to Read/Write any selected register(s).
- Commands with 2+ data bytes will operate only on an even number of bytes (these commands always transfer 16-bit words of data).

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6.9.5 Transaction Formats by Protocol Mode

Several commands use either a 3 or 4-byte address depending on a configuration setting of the target device. Several commands have a variable initial access latency that depends on a configuration setting of the target device. The length of data transfer depends on the command or operating conditions. The controller must be aware of these configuration settings and command behaviors in order to select the correct command format.

6.9.5.1 1S-1S-1S

The following transaction formats may be used in the 1S-1S-1S protocol mode:

- Format 0.A: Command only
- Format 0.B: Command and Read Data
- Format 0.C: Command, 3-byte Address, and Read Data
- Format 0.D: Command, 4-byte Address, and Read Data
- Format 0.E: Command, 3-byte Address, Initial Access Latency (Dummy Cycles), and Read Data
- Format 0.F: Command, 4-byte Address, Initial Access Latency (Dummy Cycles), and Read Data
- Format 0.G: Command and Write Data
- Format 0.H: Command and 3-byte Address
- Format 0.I: Command and 4-byte Address
- Format 0.J: Command, 3-byte Address, and Write Data
- Format 0.K: Command, 4-byte Address, and Write Data

NOTE This standard requires only a subset of the above mentioned formats. The other formats are described to ensure that if other commands are implemented in the 1S-1S-1S mode, they will follow a pre-defined format.

In figures 4 through 10, where a command modifier is used for an address, 4-Byte address is shown, but 3-Byte address may be a target device specific option enabled by default, a configuration register setting, or a command. The SFDP will indicate the availability and configuration method for 3 or 4-byte address use when SFDP is supported by the target device.

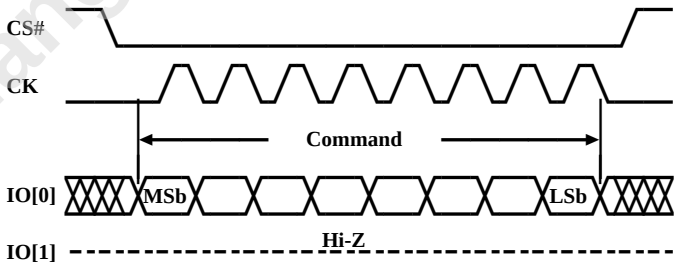

Figure 4 — 1S-1S-1S Format 0.A Command

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6.9.5.1 1S-1S-1S (cont'd)

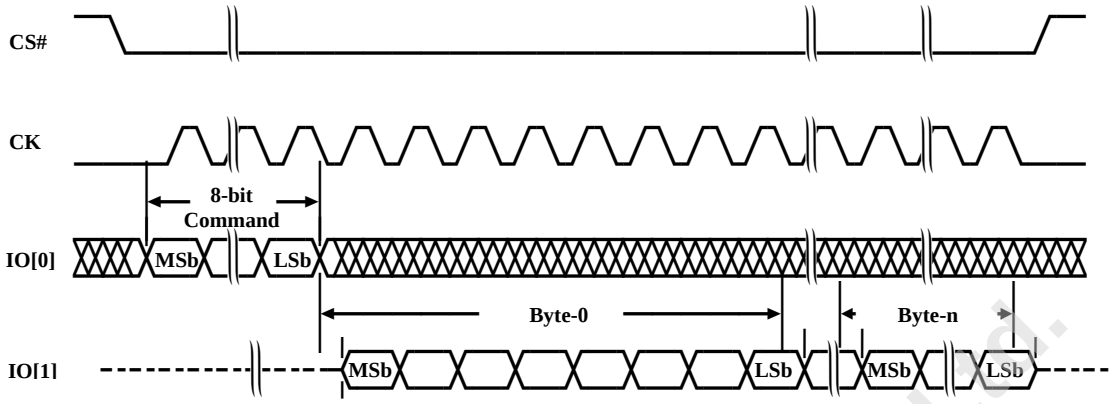

Figure 5 — 1S-1S-1S Format 0.B Command and Read Data

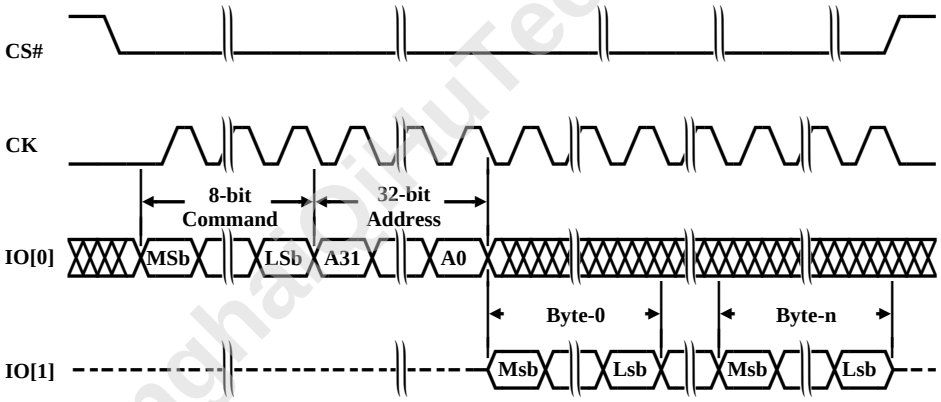

Figure 6 — 1S-1S-1S Format 0.D Command, 4-byte Address, and Read Data

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6.9.5.1 1S-1S-1S (cont'd)

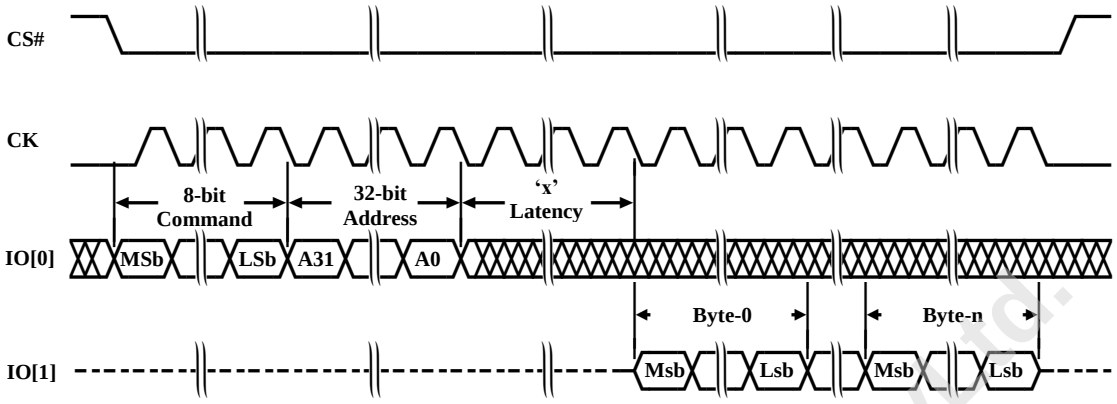

Figure 7 — 1S-1S-1S Format 0.F Command, 4-Byte Address, 'x' Latency Cycles, and Read Data

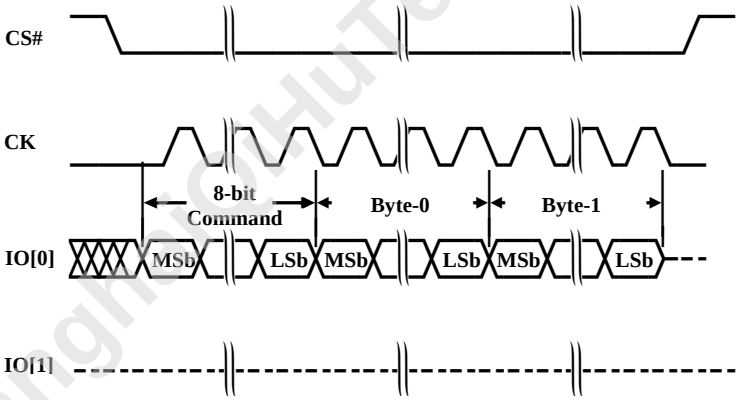

Figure 8 — 1S-1S-1S Format 0.G Command and Write Data

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6.9.5.1 1S-1S-1S (cont'd)

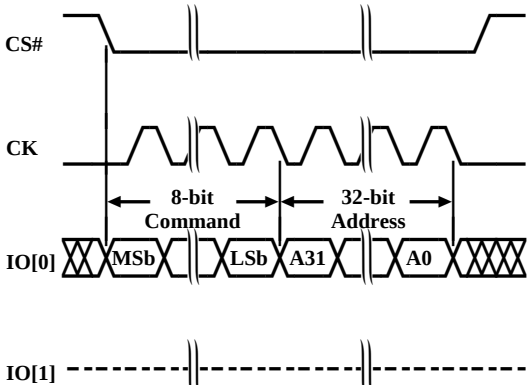

Figure 9 — 1S-1S-1S Format 0.I Command and 4-Byte Address

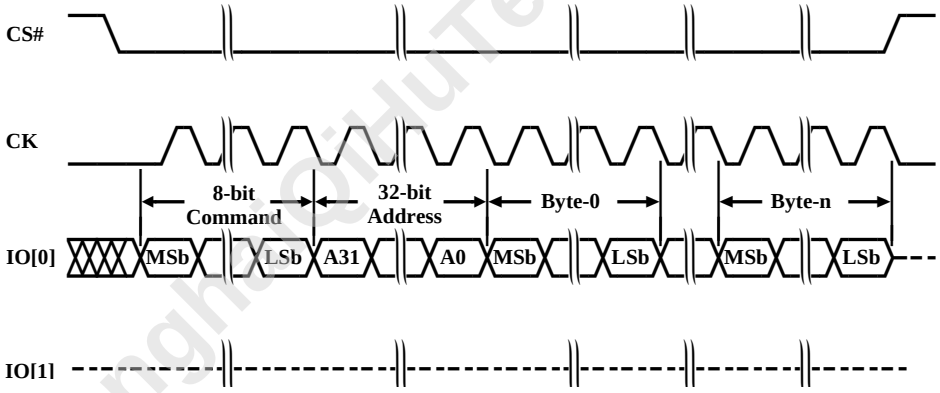

Figure 10 — 1S-1S-1S Format 0.K Command, 4-Byte Address, and Write Data

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6.9.5.2 8D-8D-8D Profile 1.0

The following transaction formats are used in Profile 1.0 mode 8D-8D-8D:

- Format 1.A: Command and Command Extension
- Format 1.B: Command, Command Extension, 4-byte Address, ‘n’ Latency Cycles, and Read Data
- Format 1.C: Command, Command Extension, and 4-byte Address
- Format 1.D: Command, Command Extension, 4-byte Address, and Write Data

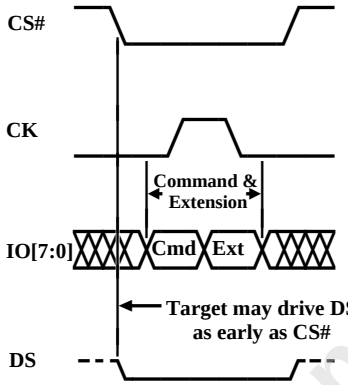
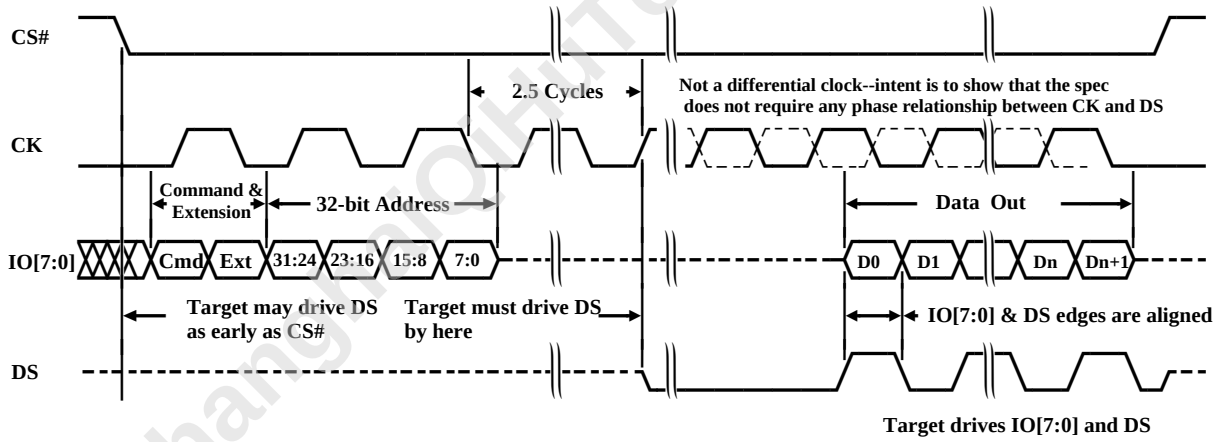


Figure 11 — Profile 1.0 8D-8D-8D Format 1.A: Command and Command Extension



NOTE 1 In most commands the modifier is a 4-byte address field as shown in the diagram. Some commands use 3-byte address. In that case the address will be sent over the first three byte of the address field indicated in the diagram starting with the most significant byte and the dummy cycle count will start with the rising edge of the clock following the third address byte. Other commands use a single byte address. In that case the address will be sent over the first byte of the address field indicated in the diagram and the dummy cycle count will start with the rising edge of the clock following that single modifier byte. Some commands have no address bytes. In that case the initial latency will start right after the command modifier. Refer to SFDP for the number of address bytes for each command.

NOTE 2 If the system supports the optional XiP Mode, the controller device may skip the command and extension and may follow the last address byte with a predefined sequence that will indicate to the target device to stay in the XiP mode for another transaction.

Figure 12 — Profile 1.0 8D-8D-8D Format 1.B: Command and Command Extension, Address, ‘x’ Latency Cycles, and Read Data

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6.9.5.2 8D-8D-8D Profile 1.0 (cont'd)

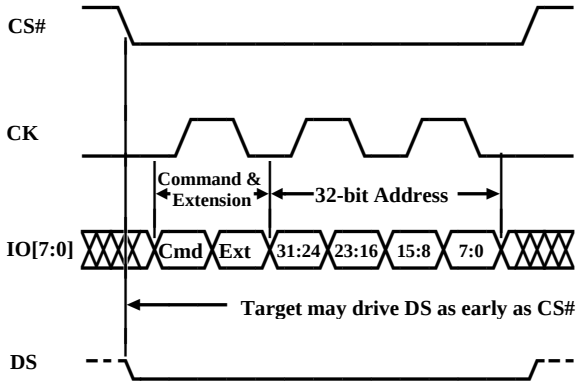
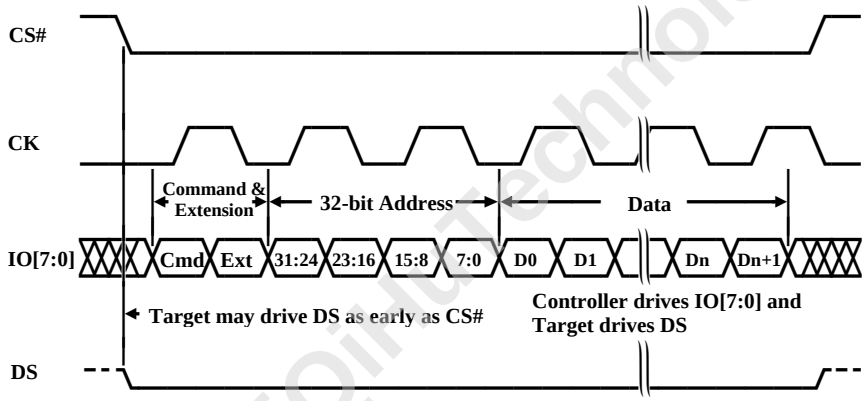


Figure 13 — Profile 1.0 8D-8D-8D Format 1.C: Command and Command Extension, Address



NOTE In most commands the modifier field is a 4-byte address field as shown in the diagram. Some commands have no address bytes. In that case the data bytes will be sent immediately after the command and the command extension bytes. Other commands use a single byte address. In that case the address will be sent over the first byte of the address field indicated in the diagram and the data bytes will be sent immediately after the address byte. Refer to SFDP for the number of address bytes for each command.

Figure 14 — Profile 1.0 8D-8D-8D Format 1.D: Command and Command Extension, Address, and Write Data

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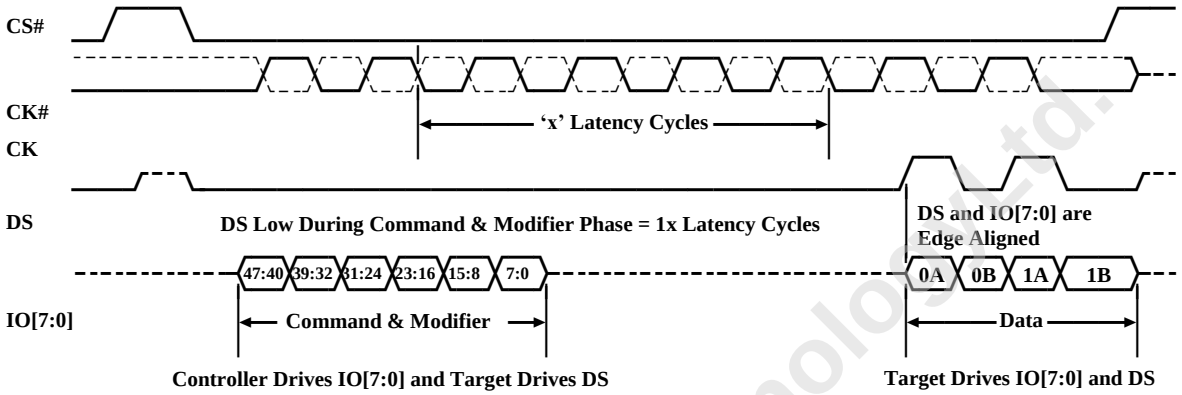
6.9.5.3 8D-8D-8D Profile 2.0

The following transaction formats are used in Profile 2.0 mode 8D-8D-8D:

- Format 2.A: Command, 5-byte Address, and Initial Access Latency
- Format 2.B: Command, 5-byte Address, and Initial Access Latency



NOTE CK# is optionally used in Profile 2.0 commands for target devices that require differential clock.

Figure 15 — Profile 2.0 8D-8D-8D Format 2.A: Command, 5-byte Address Modifier, 'x' Latency Cycles, and Read Data

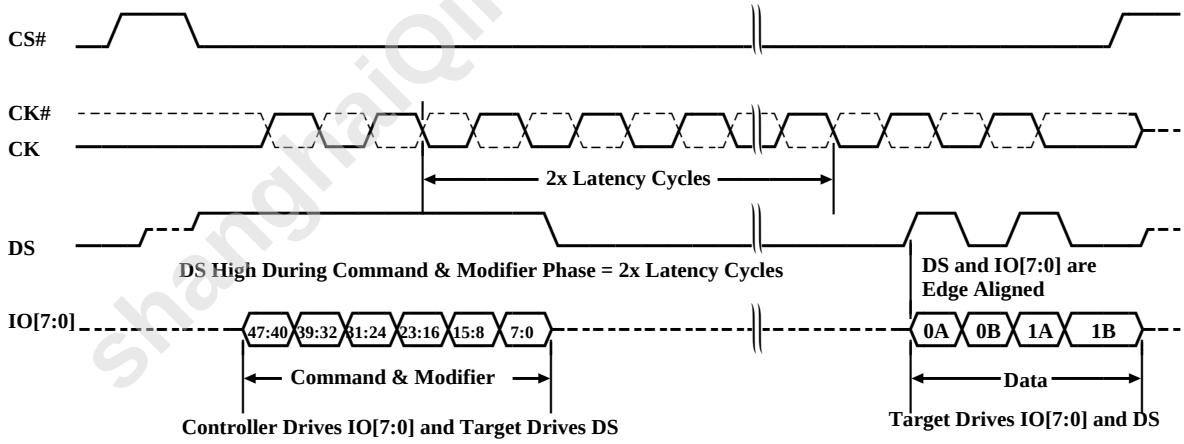


Figure 16 — Profile 2.0 8D-8D-8D Format 2.A: Command, 5-byte Address Modifier, '2x' Latency Cycles, and Read Data

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6.9.5.3 8D-8D-8D Profile 2.0 (cont'd)

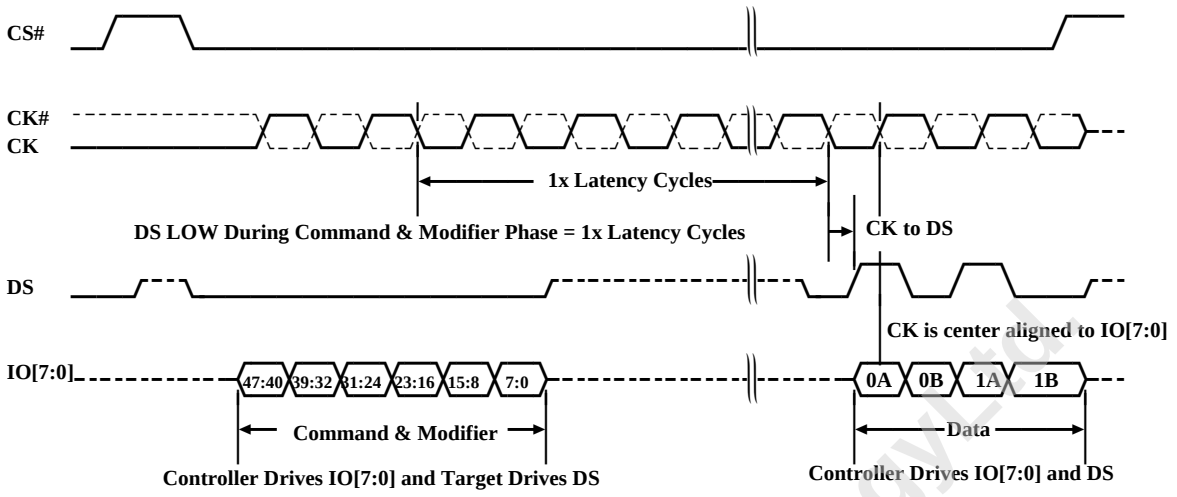

Figure 17 — Profile 2.0 8D-8D-8D Format 2.B: Command, 5-byte Address, Initial Access Latency, and Write Data

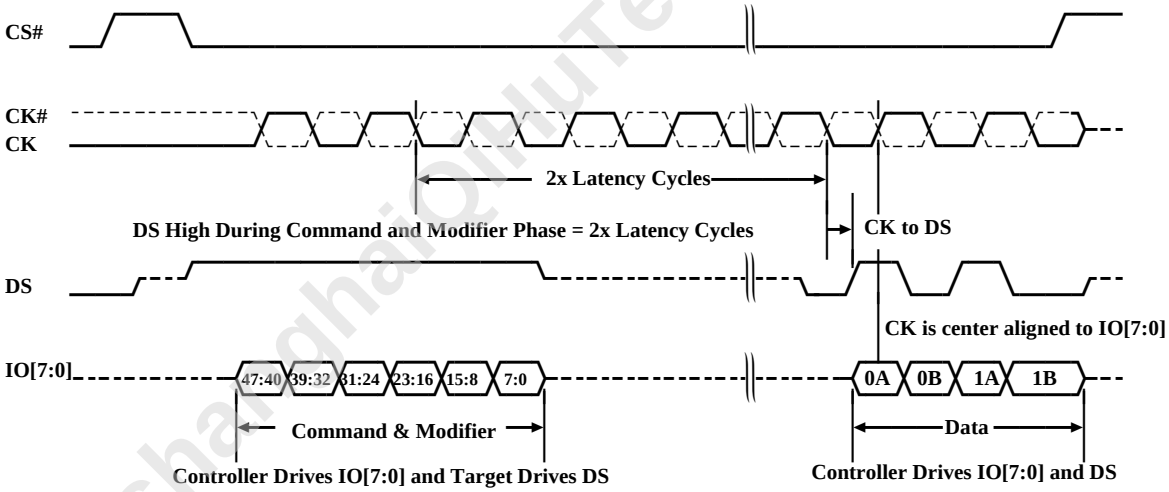

Figure 18 — Profile 2.0 8D-8D-8D Format 2.B: Command, 5-byte Address, 2x Initial Access Latency, and Write Data

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6.9.5.3 8D-8D-8D Profile 2.0 (cont'd)

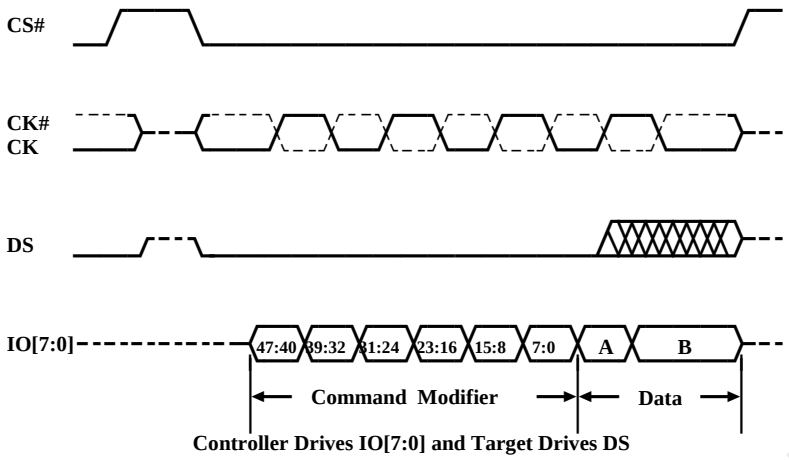

Figure 19 — Profile 2.0 8D-8D-8D Format 2.B: Command, 5-byte Address, Zero Latency, and Write Data

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6.10 Command Descriptions

6.10.1 Identification Commands

6.10.1.1 Read SFDP

The Read Serial Flash Discoverable Parameters (SFDP) command reads from a database of standard parameters stored within the xSPI target device. The format of this database and the parameters is defined in the JESD216 standard. Supporting the Read SFDP command is Preferred.

In the 1S-1S-1S protocol mode, there is no command extension, but there is a 3-byte address followed by 8 cycles of initial access latency, before data bytes are read. See Figure 7 — 1S-1S-1S Format 0.F Command, 4-Byte Address, ‘x’ Latency Cycles, and Read Data.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte and 3 or 4 bytes of address. There is an 8 or 20 cycle initial access latency. Then the target transfers 1 or more words of SFDP information to the controller. The beginning of the SFDP data stream is identified by the 4 ASCII characters for SFDP. See Figure 12 — Profile 1.0 8D-8D-8D Format 1.B: Command and Command Extension, Address, ‘x’ Latency Cycles, and Read Data.

The address selects the starting point for reading a sequence of bytes or words from the SFDP database.

6.10.2 Profile 1.0 Commands

The set of Profile 1.0 commands are intended to manage a non-volatile memory device. Most of these commands are software backward compatible with legacy SPI memory commands. In some protocol modes the commands are also signal protocol backward compatible with legacy SPI. In other protocol modes, the memory controller design must be updated to be compatible with some or all of the xSPI protocol modes while legacy SPI memory driver software may be used with little or no change in all protocol modes.

Commands that program or erase in the memory array have command modifier bytes that are used to convey a starting address within the array where the command operation is to begin. The address format is a byte address that is either 3 or 4-bytes (24-bits or 32-bits) in length. The provision of 3-byte or 4-byte address is determined by either address length mode commands or a target device specific configuration. The bytes and bits are sent in most significant to least significant order (left to right in the figures below). For DDR protocol modes in which an even number of data bytes are always transferred, the least significant bit (0) of the address is always zero.

Address Bytes and Bits																								
2								**1**								**0**							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 20 — 3-byte Address Format

Address Bytes and Bits																															
3								**2**								**1**								**0**							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 21 — 4-byte Address Format

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6.10.2 Profile 1.0 Commands (cont'd)

In some commands, the address is followed by a number of clock cycles in which no data is transferred. These cycles are used to provide time for initial access latency of the memory array and allow for the controller to stop driving IO signals and the target to start driving IO signals (bus turnaround) for read transactions. Legacy SPI protocols often described these as Dummy cycles. The number of these initial access latency cycles is configurable for most commands.

The factory default number of address bytes and latency cycles configured following POR is indicated in the SFDP. The host system must remain aware of any volatile or non-volatile reconfiguration of the number of address bytes or initial latency cycles in order to remain in protocol synchronization with the target devices. A hardware or software reset may be used to return to the POR default protocol and number of address bytes, to regain protocol mode synchronization with the target device.

Some commands convey only the command with no command modifier, latency, or data transfer. These commands cause a change in target device behavior such as enabling or disabling the program and erase commands, suspending and resuming program and erase commands, entering and exiting a low power mode, resetting the target device, or change to a different protocol mode.

Some commands read or write status or configuration registers. Some commands select the target register implicitly; other commands provide an address to select the register affected. Register formats and addressing are target device specific.

6.10.2.1 Memory Granularity

The memory array of a Flash memory xSPI target is divided into two levels of granularity comprised of sectors, and pages. A sector is the minimum size and alignment (granularity) of an area that can be erased in the data array of a Flash memory device. A Page is the maximal size and alignment (granularity) of an area that can be programmed with a single command. Sectors range in size from 4 Kbytes to 256 Kbytes and pages are 256 bytes or 512 bytes, in existing flash memories. The sizes of sectors and pages in a specific device are indicated in the SFDP.

Figure 22 shows the memory map of a Flash xSPI device:

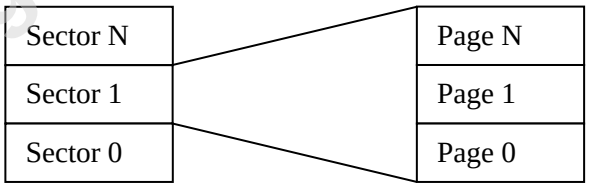

Figure 22 — xSPI Flash Memory Map

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6.10.2.2 Read Zero Latency

The Read with Zero Latency command provides an SPI backward compatible command for reading data. This command is generally used for reading initial boot code from an SPI non-volatile memory before the device is identified. This initial boot code may perform the device identification process and then select a different supported read command or protocol mode for higher performance. Because this command in legacy devices provides very little time for accessing a memory array, the required clock speed support for the command is limited to a maximum of 50 MHz. This means a target device that supports this command must be able to support the command only up to 50 MHz. Target devices may support higher clock rates for this command but that is not a requirement.

In the 1S-1S-1S protocol mode, there is no command extension, but there is a 3-byte address followed by no initial access latency, before data bytes are read. See Figure 6 — 1S-1S-1S Format 0.D Command, 4-byte Address, and Read Data.

The Read with Zero Latency command is not supported in the 8D-8D-8D protocol mode.

6.10.2.3 Read Fast

The Read Fast commands provide SPI backward compatible commands for reading data at higher clock frequencies.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte and 4 bytes of address, followed by a configurable number of initial access latency cycles. Then the target transfers 1 or more words of data to the controller. See Figure 12 — Profile 1.0 8D-8D-8D Format 1.B: Command and Command Extension, Address, ‘x’ Latency Cycles, and Read Data.

6.10.2.4 Read Wrapped Setup

The Read Wrapped Setup command provides an SPI backward compatible command for configuring the data transfer order of read commands. This command writes a data byte / word into a volatile configuration register to select linear or wrapped data transfer order and for wrapped order, also set the wrapping group alignment and length.

Linear transfer order starts with the address selected location and transfers incrementally higher address locations until the transaction is ended by driving CS# HIGH.

Wrapped transfer order starts with the address selected location and transfers incrementally higher address locations until the end of an aligned and length group of words is encountered. The transfer then continues starting at the lowest address of the same group and continues with higher address words until the transaction is ended. Thus, the transfer sequence wraps around within the aligned and length group of words. The alignment and length of the group is set by a target device configuration. Wrapped transactions are generally used for cache line refill by accessing the addressed location (critical word) first then wrapping around until the entire cache line is read.

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6.10.2.4 Read Wrapped Setup (cont'd)

Table 7 — Read Wrapped Setup Configuration Data Value Options

Transfer Order	Wrap Group Alignment and Length	Byte Data Value	Word Data Value
Reserved	Reserved	00h	xx00h
Wrap around	16 bytes	01h	xx01h
Wrap around	32 bytes	02h	xx02h
Wrap around	64 bytes	03h	xx03h
Linear	none	1xh	xx1xh

Following POR, wrap-around mode is disabled as the default state of the target device.

In the 8D-8D-8D protocol mode, for the Setup Read Wrapped command, the controller transfers the one byte command followed by a command extension byte and 4 bytes of address followed by one data byte or word that is used to configure the transfer order for the read fast or read wrapped command. Some target devices use the Read Wrapped configuration to control the transfer order of the Fast Read command. Some target devices support separate Read Fast (linear) and Read Fast Wrapped commands to enable reading in either order without changing the wrap configuration. These devices may configure the wrap through a bit-filed in a configuration register. In this case the device may perform a regular wrap or a Hybrid wrap. The SFDP will indicate the availability and configuration method for Read Wrapped Setup. See Figure 14 — Profile 1.0 8D-8D-8D Format 1.D: Command and Command Extension, Address, and Write Data.

6.10.2.5 Write Enable

The Write Enable command provides an SPI backward compatible command for enabling commands that change memory locations in the target device. Following POR, commands that change memory data are prevented from executing. The Write Enable command must precede commands to write, program or erase memory locations. The Write Enable command serves to make any memory changes a two or more command sequence to minimize the chance of an unintended change to memory data.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte. There are no additional command modifier bytes, latency or data phases. See Figure 11 — Profile 1.0 8D-8D-8D Format 1.A: Command and Command Extension.

6.10.2.6 Write Disable

The Write Disable command provides an SPI backward compatible command for disabling commands that change memory locations in the target device. Following POR, commands that change memory data are prevented from executing. The Write Enable command must precede commands to write, program or erase memory locations. The Write Disable command may be used following the end of memory changing commands to return to a state in which these commands are again prevented from executing.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte. There are no additional command modifier bytes, latency or data phases. See Figure 11 — Profile 1.0 8D-8D-8D Format 1.A: Command and Command Extension.

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6.10.2.7 Program

The Program commands provide SPI backward compatible commands for programming data into a non-volatile memory array. The program commands provide an address and writes data bytes into a programming buffer within the target device. The minimum number of bytes transferred is one byte. The maximum number of bytes transferred is one page of bytes. The page size is device specific. The page size is indicated in the SFDP. The page is aligned on a page size boundary. The address selects the starting point within the page for the data transferred. Transferring more bytes than fit in a page (going beyond the end of a page) has undefined results. Byte locations within a page that are not transferred (written) are not modified by the program command.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte. The command is followed by 4 bytes of address followed by a variable number of data words written to a programming buffer in the target device. See Figure 14 — Profile 1.0 8D-8D-8D Format 1.D: Command and Command Extension, Address, and Write Data.

6.10.2.8 Erase 4 Kbytes

The Erase 4 Kbytes command provides an SPI backward compatible command for erasing data in a non-volatile memory array. A 4 Kbyte aligned group of bytes is erased by the command. The 4 Kbyte group is selected by the command address pointing anywhere within the group.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte and 4 bytes of address. There are no latency or data transfer phases. See Figure 14 — Profile 1.0 8D-8D-8D Format 1.D: Command and Command Extension, Address, and Write Data.

6.10.2.9 Erase 32 Kbytes

The Erase 32 Kbytes command provides an SPI backward compatible command for erasing data in a non-volatile memory array. A 32 Kbyte aligned group of bytes is erased by the command. The 32 Kbyte group is selected by the command address pointing anywhere within the group.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte and 4 bytes of address. There are no latency or data transfer phases. See Figure 14 — Profile 1.0 8D-8D-8D Format 1.D: Command and Command Extension, Address, and Write Data

6.10.2.10 Erase 64+ Kbytes

The Erase 64+Kbytes command provides an SPI backward compatible command for erasing data in a non-volatile memory array. An erase size aligned group of bytes is erased by the command. The group is selected by the command address pointing anywhere within the group. The size of the erase group is 64 Kbytes or more. The size of the erase group is device specific. The group size is indicated in the SFDP.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte and 4 bytes of address. There are no latency or data transfer phases. See Figure 13 — Profile 1.0 8D-8D-8D Format 1.C: Command and Command Extension, Address.

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6.10.2.11 Erase Chip

The Erase Chip command provides an SPI backward compatible command for erasing data in a non-volatile memory array. The entire memory array of the target device is erased by the command. The device (chip) memory array size is indicated in the SFDP.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte. There are no additional command modifier bytes, latency or data phases. See Figure 11 — Profile 1.0 8D-8D-8D Format 1.A: Command and Command Extension.

6.10.2.12 Program / Erase Suspend

The Program / Erase Suspend command provides an SPI backward compatible command for suspending the progress of commands that change memory locations in the target device. Program and erase operations are relatively long time frame activities. The suspend command allows temporarily stopping the operation in order to perform a read of memory or do a program of data during a long background erase operation in another sector.

The time to complete the suspend operation is device specific but the target device status register may be read repeatedly (polled) to determine when the device is no longer busy with the program or erase command. After the program or erase operation is suspended, the following commands may be executed if they are supported by the device for use during a suspend condition.

Profile 1.0 Commands that can execute during suspend:

Read Zero Latency, Read Fast, Read Wrapped, Read Wrapped Setup, Program, Erase 4Kbytes, Erase 32Kbytes, Erase 64+Kbytes, Program / Erase Resume, Read Status Register, Read Register, Write Status Register, Write Register, Enter Deep Power Down, Exit Deep Power Down, Soft Reset, Reset Enable, Soft Reset and Enter default protocol mode, and Enter default protocol mode.

Whether a:

- program command may be executed during an erase suspend;
- an erase command may be executed during a program suspend;
- program command may be executed during a program suspend;
- or an erase command may be executed during an erase suspend;
- is device specific.

The supported suspend options are indicated in the SFDP.

It is recommended to not reset the target device during a suspended program or erase as this may leave a portion of the memory array in an unknown state that will require the area of memory to be erased to return it to a known state.

The allowed command options during suspend are indicated in the SFDP.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte. There are no additional command modifier bytes, latency or data phases. See Figure 11 — Profile 1.0 8D-8D-8D Format 1.A: Command and Command Extension.

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6.10.2.13 Program / Erase Resume

The Program / Erase Resume command provides an SPI backward compatible command for resuming the progress of a command that has been suspended. In the case of nested suspended operations, e.g., a suspended program operation during a suspended erase operation, the most recently suspended operation is resumed.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte. There are no additional command modifier bytes, latency or data phases. See Figure 11 — Profile 1.0 8D-8D-8D Format 1.A: Command and Command Extension.

6.10.2.14 Read Status Register

The Read status register command provides an SPI backward compatible command for reading target device status. This command implicitly selects the status register for read. A single byte register is read out. If the transaction continues to read more bytes the same status register is repeatedly read out. The format of the status information is device specific. The status register format is indicated in the SFDP.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte and 4 bytes of address. There is a configurable initial access latency. Then the target transfers 1 or more words of data to the controller. The status register content is repeated in both bytes of the data word. See Figure 12 — Profile 1.0 8D-8D-8D Format 1.B: Command and Command Extension, Address, ‘x’ Latency Cycles, and Read Data.

6.10.2.15 Read Register

The Read Register command provides for reading an address selected register. The register address map and register formats are target device specific. The supported map and formats are indicated in the SFDP. Only a single byte register is read. If the transaction reads more than one byte / word the same register is repeated.

In the 8D-8D-8D protocol modes, the controller transfers the one byte command followed by a command extension byte and 4 bytes of address followed by a configurable number of initial access latency cycles. Then the target transfers 1 or more words of register data to the controller. The status register content is repeated in both bytes of the data word. See Figure 12 — Profile 1.0 8D-8D-8D Format 1.B: Command and Command Extension, Address, ‘x’ Latency Cycles, and Read Data.

6.10.2.16 Write Status and Configuration Registers

The Write Status-Cfg Register command provides an SPI backward compatible command for writing the status and configuration register(s). This command either implicitly selects the status and configuration registers for write or uses an address field for this selection. The format of the status and configuration information is device specific. The register formats are indicated in the SFDP. The Write Enable command must precede the Write Status and Configuration Registers command so that writing of registers is enabled.

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6.10.2.16 Write Status and Configuration Registers (cont'd)

In the 8D-8D-8D protocol modes, the controller transfers the one byte command followed by a command extension byte and optionally 4 bytes of address followed by one or more data word that is used to write either the status register or the configuration register. If there is no address, the data byte writes the status register. If the address is zero, the status register is written. If the address is one, the configuration register is written. The first received byte of the data word is used to write the selected register. The address length is indicated in the SFDP. See Figure 14 — Profile 1.0 8D-8D-8D Format 1.D: Command and Command Extension, Address, and Write Data.

6.10.2.17 Write Register

The Write Register command provides for writing an address selected register. The register address map and register formats are target device specific. Only a single byte register is written. If the transaction writes more than one byte / word only the first byte received is used to write the register. The Write Enable command must precede the Write Register command so that writing of registers is enabled.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte and one or 4 bytes of address followed by one data word written to the selected register. See Figure 14 — Profile 1.0 8D-8D-8D Format 1.D: Command and Command Extension, Address, and Write Data.

6.10.2.18 Enter Deep Power Down

The Enter Deep Power Down command provides an SPI backward compatible command for entering a low power mode. The time to enter the low power mode and therefore the time required before an Exit Deep Power Down command can be accepted is target device specific. The time required to enter deep power down is indicated in the SFDP.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte. There are no additional command modifier bytes, latency or data phases. See Figure 11 — Profile 1.0 8D-8D-8D Format 1.A: Command and Command Extension

6.10.2.19 Exit Deep Power Down

The Exit Deep Power Down command provides an SPI backward compatible command for exiting a low power mode. The time to exit the low power mode and therefore the time required before another command can be accepted is target device specific. The time required to exit deep power down is indicated in the SFDP.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte. There are no additional command modifier bytes, latency or data phases. See Figure 11 — Profile 1.0 8D-8D-8D Format 1.A: Command and Command Extension.

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6.10.2.20 Soft Reset and Enter Default Protocol Mode

The Soft Reset commands provide alternate SPI backward compatible commands for resetting a target device to a state similar to the state following POR. The only difference between a software reset and a hardware reset initiated by external signals is that a software reset does not disable any data protection features that are locked-down until a loss of power. A hardware reset returns all device state to the conditions following POR. Following the execution of a Soft Reset command, the target device is operating in its currently configured default protocol mode. Some devices allow the default protocol mode to be non-volatile configured to a mode different from the one configured when the device is first shipped from its manufacturer's factory. The factory default protocol mode is indicated in the SFDP. Host systems must remain aware of any changes to the POR default protocol mode. The time to return to the default protocol mode is indicated in the SFDP.

When the Soft Reset F0h is available, the command performs only a soft reset without entering the default protocol mode. A two command sequence option may be available: 66h followed by 99h. That sequence performs both a soft reset and enters the default protocol mode.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte. There are no additional command modifier bytes, latency or data phases. See Figure 11 — Profile 1.0 8D-8D-8D Format 1.A: Command and Command Extension.

6.10.2.21 Enter Another Protocol Mode

The Enter Another Protocol Mode commands provide alternate SPI backward compatible commands for switching to a different protocol mode. Command options may be available for entering 8D-8D-8D. The 1S-1S-1S mode is recommended as the default POR mode so that a software or hardware reset will return to the 1S-1S-1S mode. The time to enter another protocol mode is device dependent and is indicated in the SFDP.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte. There are no additional command modifier bytes, latency or data phases. See Figure 11 — Profile 1.0 8D-8D-8D Format 1.A: Command and Command Extension.

Some devices transfer protocol modes by writing to a register. The method to change protocol modes is indicated in SFDP.

6.10.2.22 Read Flag Status Register

The Read flag status register command provides command for reading target device operation flag status. This command implicitly selects the flag status register for read. A single byte register is read out. If the transaction continues to read more bytes, the same status register is repeatedly read out.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte. There is an initial access latency. Then the target transfers 1 or more words of data to the controller. The flag status register content is repeated in both bytes of the data word.

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6.10.2.23 Clear Flag Status Register

The Clear flag status register command provides command for clearing target device operation flag status.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte. See Figure 11 — Profile 1.0 8D-8D-8D Format 1.A: Command and Command Extension.

6.10.2.24 Read Volatile / NV Register

The Read Volatile/NV Register commands provide for reading an address selected Volatile or NV register. The register address map and register formats are target device specific. The supported map and formats are indicated in the SFDP. Only a single byte register is read. If the transaction reads more than one byte / word the same register is repeated.

In the 8D-8D-8D protocol modes, the controller transfers the one byte command followed by a command extension byte and 4 bytes of address followed by an initial access latency cycles indicated by SFDP. Then the target transfers 1 or more words of register data to the controller. The status register content is repeated in both bytes of the data word. See Figure 12 — Profile 1.0 8D-8D-8D Format 1.B: Command and Command Extension, Address, ‘x’ Latency Cycles, and Read Data.

6.10.2.25 Write Volatile / NV Register

The Write Volatile/NV Register commands provide for writing an address selected Volatile or NV register. The register address map and register formats are target device specific. Only a single byte register is written. If the transaction writes more than one byte / word only the first byte received is used to write the register. The Write Enable command must precede the Write Register command so that writing of registers is enabled.

In the 8D-8D-8D protocol mode, the controller transfers the one byte command followed by a command extension byte and 4 bytes of address followed by one data word written to the selected register. See Figure 14 — Profile 1.0 8D-8D-8D Format 1.D: Command and Command Extension, Address, and Write Data.

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6.10.3 Profile 2.0 Commands

The set of Profile 2.0 commands provide a means to read or write data with any type of target device. The meaning of the data is device specific. Target devices using Profile 2.0 commands may for example support:

- non-volatile memory arrays such as NOR Flash, NAND Flash, FRAM, or nvSRAM;
- volatile memory arrays such as SRAM, PSRAM, or DRAM;
- register mapped Input/Output functions such as graphics or network adapters, sensors, etc.;
- or programmable function devices such as Field Programmable Gate Arrays (FPGA).

The Profile 2.0 commands are available only in 8D-8D-8D protocol mode.

The Profile 2.0 commands provide options for:

- Command selected read or write;
- Command selected access to two separate address spaces referred to as memory or register space;
- Command selected data transfer order in two options referred to as linear or wrapped.

Each transaction begins with CS# going LOW. The Profile 2.0 command then identifies the transaction as a read or a write; to the memory or register address space; in linear or wrapped transfer order. The command is followed by a 5-byte command modifier that is used as a 40-bit word address into either the memory or register address space. The command modifier is followed by a configurable initial access latency phase, then the data transfer phase that continues until the transaction is ended by CS# returning to HIGH.

Linear transfer order starts with the address selected location and transfers incrementally higher address word locations until the transaction is ended by driving CS# HIGH.

Wrapped transfer order starts with the address selected location and transfers incrementally higher word address locations until the end of an aligned and length group of words is encountered. The transfer then continues starting at the lowest address of the same group and continues with higher address words until the transaction is ended. Thus, the transfer sequence wraps around within the aligned and length group of words. The alignment and length of the group is set by a device configuration. Wrapped transactions are generally used for cache line refill by accessing the addressed location (critical word) first then wrapping around until the entire cache line is read.

An optional configuration may be available to combine one complete wrapped transfer of a group immediately followed by linear transfer starting at the lowest address of the next higher address group. This is referred to as a Hybrid Wrapped transaction. Hybrid wrapped transactions can combine an initial wrapped access for a cache line with the linear pre-fetch of the next sequential cache line, without the need to send two separate commands.

Each Profile 2.0 command transaction independently selects the transfer order, so wrapped and linear order accesses for code cache line refill or linear data block transfers can be interleaved as needed without a need to reconfigure the transfer order in between each command as is required in the 1S-1S-1S protocol Profile 1.0 command set.

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6.10.3.1 Command Modifier Format

The 5 bytes of command modifier are used to provide up to a 40-bit address to select the initial 16-bit word location in the command selected address space. The first (high order) 3 bytes of address provide enough address resolution to initiate an access within the target device.

The last two bytes of the command modifier select the first data word location to be transferred. These two bytes of command modifier may also provide control bits for the transaction that further modify the command behavior but are not needed to initiate the access within the target device.

The format of (meaning the bits within) the command modifier is device specific and is indicated in the SFDP. The standard defined formats are:

Table 8 — Profile 2.0 Command Modifier Formats

Format	Command Bits							
	0							
	47	46	45	44	43	42	41	40
2	Command							
	R/W	R/M	L/W	1	1	1	1	1

Format	Command Modifier Bytes and Bits																																			
	4								3								2								1								0							
	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	Word Address Bits																																							
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	Reserved													2	1	0

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6.10.3.1 Command Modifier Format (cont'd)

Table 9 — Command and Modifier Bit Description

Bit	Bit Name	Bit Function
47	R/W#	Identifies the transaction as a read or write. R/W#=1 indicates a Read transaction R/W#=0 indicates a Write transaction
46	Address Space (AS)	Indicates whether the read or write transaction accesses the memory or register space. AS=1 indicates the register space AS=0 indicates memory space The register space is used to access target ID and Configuration registers.
45	Burst Type	Indicates whether the burst will be linear or wrapped. Burst Type=1 indicates linear burst Burst Type=0 indicates wrapped burst
44-40	Command Extension	Command extension – 11111b These reserved bits must be set to 1 by the controller interface
39-16	Row and Upper Column Address	Row and Upper Column component of the target address: System word address bits A31-A3 Any upper Row address bits not used by a particular device density should be set to 0 by the controller interface. The size of Rows and therefore the address bit boundary between Row and Column address is target device dependent.
15-3	Reserved	Reserved for future column address expansion. Reserved bits are don't care in current devices but should be set to 0 by the controller interface for future compatibility.
2-0	Lower Column Address	Lower Column component of the target address: System word address bits A2-0 selecting the starting word.

6.10.3.2 Read Commands

All Profile 2.0 Read commands follow the same signaling protocol. (Figure 15 and Figure 16)

6.10.3.2.1 Read Register Wrapped

The Read Register Wrapped command reads data from the register address space in wrapped order.

6.10.3.2.2 Read Register Linear

The Read Register Linear command reads data from the register address space in linear order.

6.10.3.2.3 Read Memory Wrapped

The Read Register Wrapped command reads data from the memory address space in wrapped order.

6.10.3.2.4 Read Memory Linear

The Read Memory Linear command reads data from the memory address space in linear order.

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6.10.3.3 Write Commands

All Profile 2.0 write commands follow one of two transaction formats; either write with initial latency or write with zero initial latency. The transaction format used may be target device specific or address space specific. A target device may always use the same transaction format or may use one format for memory address space and the other for register address space. The write transaction format supported for memory and register space is indicated in the SFDP.

In write transactions with initial latency, the target drives DS during the command and command modifier phases to indicate whether one or two latency cycle counts are needed by the target before the controller begins data transfers. During the initial latency the target stops driving DS and the controller begins driving DS as a write mask indication. The initial latency count is used a turnaround time for the DS signal between target and controller drive of the DS signal.

Writes with zero initial latency, do not have a turnaround period for DS. The target device will always drive DS during the command and command modifier period to indicate whether extended latency is required for that transaction. However, the DS is driven before the target device has received the first byte of command, that is, before the target knows whether the transaction is a read or write, to memory space or register space. In the case of a write with zero latency, the DS state during the command and command modifier period does not affect the initial latency of zero. Since controller write data immediately follows the command and command modifier phases in this case, the target may continue to drive DS LOW or may take DS to High-Z during write data transfer. The controller must not drive DS during Writes with zero latency. Writes with zero latency do not use DS as a data mask function. All bytes of write data are written (full word writes).

Figure 17 and Figure 18 for write with initial latency. Figure 19 for write with zero initial latency.

6.10.3.3.1 Write Register Wrapped

The Write Register Wrapped command writes data to the register address space in wrapped order.

6.10.3.3.2 Write Register Linear

The Write Register Linear command writes data from to the register address space in linear order.

6.10.3.3.3 Write Memory Wrapped

The Write Memory Wrapped command writes data to the memory address space in wrapped order.

6.10.3.3.4 Write Memory Linear

The Write Memory Linear command writes data to the memory address space in linear order.

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6.10.3.4 Enter Default Protocol Mode (1S-1S-1S)

The Enter Default Protocol Mode command is a sequence of three Write Register Linear commands that write to register space are required. The first Write Register Linear command has a 00555h command modifier value, and one word of 00AAh data. The second Write Register Linear command has a 002AAh command modifier value, and one word of 0055h data. The third Write Register Linear command has a 00555h command modifier value, and one word of 00F5h data. This transaction sequence causes a return to the default protocol mode. The time to return to the default protocol mode is device dependent and is indicated in the SFDP.

6.10.3.5 Data Strobe Options

6.10.3.5.1 Deterministic Latency

Target devices may provide deterministic latency behavior in which the clock cycle count of any latency is well defined for both the controller and the target.

- The device design may provide fixed latencies that are always consistent.
- Or, the latencies may be configurable by device control registers to count clock cycles.
- Or, the Data Strobe (DS) may indicate whether a fixed or configured latency is extended by defined increments in certain cases.
- Or, additional latency may be inserted after the start of data transfer at known address boundaries with the amount of latency determined based on the starting address of the transaction or on the location of the address boundary

The initial access latency fixed by the design or by the device manufacturer factory configuration is indicated in the SFDP. The host system must remain aware of any later reconfiguration of the initial access latency.

DS may be driven by the target during the command and command modifier phases to indicate whether the target needs an additional latency period equal to the fixed or configured initial access latency. Normally DS is LOW during the command and command modifier phases to indicate that only the fixed or configured initial access latency is needed before the start of data transfer. However, in some cases the target may drive DS HIGH during the command and command modifier phases to indicate that an additional count of the initial access latency will be required before the start of data transfer. Following the command and command modifier phases during a read transaction the DS may be driven LOW or not driven to return to a High-Impedance (Hi-Z) state. If the target device uses the DS as a write mask input during write transactions, following the command and command modifier phases, during a write transaction, the DS must not be driven and return to a High-Impedance (Hi-Z) state, in order to allow for the DS signal to turn around from the target driving to controller driving. Whether DS is used by the target for indicating the need for additional initial access latency or as a write data mask is indicated in the SFDP.

Additional latency may be inserted after the start of data transfer at certain address boundaries. The amount of latency may be based on the starting address and the configured initial access latency count or on the boundary location. Boundary related latency insertion behavior is indicated in the SFDP.

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6.10.3.5.2 Variable Latency

During read transactions the controller may choose to use the DS signal as the sole way to recognize the target insertion of initial access latency or additional latency after the beginning of data transfer. While DS is LOW, data is not transferred. Data is only transferred relative to the next rising and falling edge of DS. CK and therefore DS are required to rise and fall during each CK cycle that data is transferred such that full words are always minimum transfer size. If the target maintains DS LOW throughout a clock (CK) cycle, the target is inserting additional latency in the data transfer. A controller using DS as the sole indicator of read latency is relieved of the need to track and count deterministic latency periods. The controller simply captures data relative to DS transitions and the target inserts latency as needed by the target.

During write transactions DS may or may not be driven by the target and does not provide a CK cycle by cycle indication of data transfer acceptance. As described in the Profile 2.0 commands Deterministic Latency clause, if DS is driven by the target during the command and command modifier phases, DS is used as an indication of requirement for an additional initial access latency count before the start of data transfer. This serves as a limited form of variable initial access latency for a write transaction. Use of DS for variable initial latency is indicated in the SFDP.

After the start of write data transfer, DS may be used as a write data mask signal from the controller and is not available for latency (flow) control by the target. The controller must be aware of any limitations on the length of write data transfers to the target. Write length limitations are indicated in the SFDP.

6.10.3.5.3 Write Data Mask

The target may use DS during the data transfer phase as a byte write data mask input. All Profile 2.0 commands use the 8D-8D-8D protocol mode and therefore always transfer full words of data in read and write transactions. However, some systems need byte resolution control over write operations in a memory. This is often used in volatile memory types. If DS is used as a byte write data mask: when DS is LOW during a byte transfer, the byte is written to memory, when DS is HIGH during a byte transfer the byte is not written to memory (masked).

The use or not of DS as a write data mask is indicated in the SFDP.

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6.10.4 Profile 2.0 Commands with Extended Command Modifier

An xSPI compliant device, that supports only the Profile 2.0 command set in the 8D-8D-8D protocol mode, has the option to implement a modified Profile 2.0 command set that reduces the command related bits and extends the command modifier bits into the command byte. This increases the number of command byte values that are used by the Profile 2.0 command set. All other aspects of the Profile 2.0 command related signal protocol and command descriptions remain the same. Only the command and command modifier format changes.

The command is reduced to the 3 high order bits of the first (command) byte. The lower 5 bits of that byte become additional upper bits of command modifier, making the command modifier 45 bits in length.

The command bits indicate Read or Write, to Register or Memory space, in Linear or Wrapped order.

The command modifier may be used to provide up to a 45-bit address to select the initial 16-bit word location in the command selected address space. The first (high order) 29-bits of address provide enough address resolution to initiate an access within the target device.

The last two bytes of the command modifier select the first data word location to be transferred. These two bytes of command modifier may also provide control bits for the transaction that further modify the command behavior but are not needed to initiate the access within the target device.
The format of (meaning of the bits within) the command modifier is target device specific and is indicated in the SFDP. The standard defined formats are:

Table 10 — Profile 2.0 Command with Extended Modifier Format

Format	Command and Upper Modifier Byte and Bits							
	5							
	47	46	45	44	43	42	41	40
2	Command			Word Address Bits				
	R/W	R/M	L/W	31	30	29	28	27

Format	Command Modifier Bytes and Bits																																					
	4								3								2								1								0							
	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	Word Address Bits																																							
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	Reserved For Future Use												2	1	0	

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6.10.4 Profile 2.0 Commands with Extended Command Modifier (cont'd)

Table 11 — Command and Modifier Bit Descriptions – HB1 Format

Bit	Bit Name	Bit Function
47	R/W#	Identifies the transaction as a read or write. R/W#=1 indicates a Read transaction R/W#=0 indicates a Write transaction
46	Address Space (AS)	Indicates whether the read or write transaction accesses the memory or register space. AS=1 indicates the register space AS=0 indicates memory space The register space is used to access target ID and Configuration registers.
45	Burst Type	Indicates whether the burst will be linear or wrapped. Burst Type=1 indicates linear burst Burst Type=0 indicates wrapped burst
44-16	Row and Upper Column Address	Row and Upper Column component of the target address: System word address bits A31-A3 Any upper Row address bits not used by a particular device density should be set to 0 by the controller interface. The size of Rows and therefore the address bit boundary between Row and Column address is target device dependent.
15-3	Reserved	Reserved for future column address expansion. Reserved bits are do not care in current devices but should be set to 0 by the controller interface for future compatibility.
2-0	Lower Column Address	Lower Column component of the target address: System word address bits A2-0 selecting the starting word.

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6.10.4 Profile 2.0 Commands with Extended Command Modifier (cont'd)

Table 12 — Commands with Extended Command Modifier Used in 8D-8D-8D Protocol Profile 2.0 Mode

Command Function	Command	Category	Additional Command Modifier Bytes	Initial Latency (CK Cycles)	Data Bytes	Command Extension Required	Req. Max. Freq. (MHz)
Read Register Wrapped	C0 to DF	3	5	1+	2+	0	
Read Register Linear	E0 - FF	3	5	1+	2+	0	
Read Memory Wrapped	80 - 9F	3	5	1+	2+	0	
Read Memory Linear	A0 - BF	3	5	1+	2+	0	
Write Register Wrapped	40 - 5F	3	5	0+	2+	0	
Write Register Linear	60 - 7F	3	5	0+	2+	0	
Write Memory Wrapped	00 - 1F	3	5	0+	2+	0	
Write Memory Linear	20 -3F	3	5	0+	2+	0	
Write Enable 1 (WREN1)	20 - 3F	3	5 "00555h"	0+	2 "00AAh"	0	
Write Enable 2 (WREN2)	20 - 3F	3	5 "002AAh"	0+	2 "0055h"	0	
Status Register Enable	20 - 3F	3	5 "00555h"	1+	2 "0070h"	0	
Status Register Read	A0 - BF	6	5	1+	2	0	
Status Register Clear	20 - 3F	3	5 "00555h"	0	2 "0071h"	0	
Enter Deep Power Down Mode	20 - 3F	4	5	0	2 "00B9h"	0	
Configuration Register Load (Volatile)	20 - 3F	4	5 "00555h"	0	2 "0038h"	1	
Configuration register Load (Volatile) - Extension	20 - 3F	5	5	0	2	0	
Configuration Register Read (Volatile)	20 - 3F	4	5 "00555h"	0	2 "00C7h"	1	
Configuration Register Read (Volatile) – Extension	A0 - BF	5	5	0	2	0	
Configuration Register Program (Non-Volatile)	20 - 3F	4	5 "00555h"	0	2 "0039h"	1	
Configuration Register Program (Non-Volatile) - Extension	20 - 3F	5	5	0	2	0	
Configuration Register Erase (Non-Volatile)	20 - 3F	4	5 "00555h"	0	2 "00C8h"	0	
Configuration Register Read (Non-Volatile)	20 - 3F	4	5 "00555h"	0	2 "00C6h"	1	
Configuration Register Read (Non-Volatile) – Extension	A0 - BF	5	5	0	2	0	
Word Program	20 - 3F	4	5 "00555h"	0	2 "00A0h"	1	
Word Program – Extension	20 - 3F	5	5	0	2	0	
Write to Buffer – 256B	20 - 3F	4	5 "SA[1]"	0	2 "0025h"	1	
Write to Buffer – 256B – Extension 1	20 - 3F	5	5	0	2 "WC[2]"	1	

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Table 12 — Commands with Extended Command Modifier Used in 8D-8D-8D Protocol Profile 2.0 (cont'd)

Command Function	Command	Category	Additional Command Modifier Bytes	Initial Latency (CK Cycles)	Data Bytes	Command Extension Required	Req. Max. Freq. (MHz)
Write to Buffer – 256B – Extension 2	20 - 3F	5	5	0	2	1+	
Program Write to Buffer (Confirm)	20 - 3F	3	5 "SA[1]"	0+	2 "0029"	0	
Sector Erase	20 - 3F	4	5 "00555h"	0	2 "0080h"	1	
Sector Erase – Extension 1	20 - 3F	5	5	0	2 "00AAh"	1	
Sector Erase – Extension 2	20 - 3F	5	5	0	2 "0055h"	1	
Sector Erase – Extension 3	20 - 3F	5	5 "SA[1]"	0	2 "0030h"	0	
Chip Erase	20 - 3F	4	5 "00555h"	0	2 "0080h"	0	
Chip Erase – Extension 1	20 - 3F	5	5	0	2 "00AAh"	1	
Chip Erase – Extension 2	20 - 3F	5	5	0	2 "0055h"	1	
Chip Erase – Extension 3	20 - 3F	5	5 "00555h"	0	2 "0010h"	0	
Erase Suspend	20 - 3F	3	5	0+	2 "00B0"	0	
Erase Resume	20 - 3F	3	5	0+	2 "0030"	0	
Program Suspend	20 - 3F	3	5	0	2 "0051h"	0	
Program Resume	20 - 3F	3	5	0	2 "0050h"	0	
Read SFDP	20 - 3F	4	5 "00555h"	0	2 "0090h"	1	
Read SFDP – Extension	A0 - BF	5	5	0	2+	0	
Enter Default Protocol Mode	20 - 3F	4	5 "00555h"	0	2 "00F5h"	0	

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7 xSPI Mechanical

7.1 Introduction

This chapter provides signal assignments to package terminal (package footprint) and package physical dimensions' options for xSPI target devices. Controller device footprints and physical dimensions are beyond the scope of the standard.

7.2 Signal Descriptions

Active LOW signal names have a hash symbol (#) suffix.

Table 13 — xSPI Signals (Normative)

Signal Name	Type	Description
CS#/ CS1#	Controller Output / Target Input	**Chip Select.** Bus transactions are initiated with a HIGH to LOW transition. Bus transactions are terminated with a LOW to HIGH transition. When a second optional x8 IO target device exists within the same package, CS1# is used for device #1 and CS2# is used for device #2.
CK/ CK1	Controller Output / Target Input	**Clock.** Command, Address and Data information is transferred from controller to target interface devices with respect to the rising or falling edge of the CK. The clock is not required to be free-running. When a second optional x8 IO target device exists within the same package, CK1 is used for device #1 and CK2 is used for device #2.
CK#/ CK1#	Controller Output / Target Input	**Clock#.** Command, Address and Data information is transferred from controller to target interface devices with respect to the crossing of CK and CK# (for devices requiring differential clock). The differential clock is not required to be free-running. When a second optional x8 IO target device exists within the same package, CK1# is used for device #1 and CK2# is used for device #2. NOTE: CK# is required in 8D-8D-8D profile 2.0 mode, but optional in profile 1.0 mode. Target devices are not required to use CK#. However, differential clock may be required by some devices for operation at greater than 100Mhz. The 1S-1S-1S mode operates on any xSPI target device without a need for CK#.
IO[7:0]	Input / Output	**Data Input/Output.** Command, Address, and Data information is transferred on these signals during Read and Write transactions.
DS/ DS1	Input / Output	**Data Strobe.** Target to controller strobe signal to capture read data sent by the target. Target to controller signal to indicate additional initial access latency needed by the target. Controller to target signal to indicate masking of individual bytes within write data words. DS initial latency indication and write data mask behavior is used by a limited subset of xSPI commands. When a second optional x8 IO target device exists within the same package, DS1 is used for device #1 and DS2 is used for device #2.
V_{DD}	Power Supply	**Core Power.**
$V_{DD}Q$	Power Supply	**Input / Output Power.**
V_{SS}	Power Supply	**Core Ground.**
$V_{SS}Q$	Power Supply	**Input / Output Ground.**

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7.2 Signal Descriptions (cont'd)

Table 14 — xSPI Optional Signals (Informative)

Signal Name	Type	Description
IO[15:8]	Input / Output	**Data Input/Output.** Optional Data information is transferred on these signals during Read and Write transactions.
CK2	Controller Output / Target Input	**Clock.** Command, Address and Data information is transferred from controller to optional second x8 IO target interface devices with respect to the rising or falling edge of the CK2. The clock is not required to be free-running.
CK2#	Controller Output / Target Input	**Clock#.** Command, Address and Data information is transferred from controller to optional second target interface devices with respect to the crossing of CK2 and CK2# (for devices requiring differential clock). The differential clock is not required to be free-running. NOTE CK2# is required in an optional second x8 IO target in 8D-8D-8D profile 2.0 mode, but optional in profile 1.0 mode. Target devices in profile 1.0 mode are not required to use CK2#. However, differential clock may be required by some devices for operation at greater than 100Mhz. The 1S-1S-1S mode operates on any xSPI target device without a need for CK#.
`	Controller Output / Target Input	**Chip Select 2.** Optional second chip select for a second x8 IO target device within the same package.
RESET#	Controller Output / Target Input	**Hardware Reset.** When LOW, the target device will self-initialize and return to the array read state. RWDS/DS and DQ[7:0] are placed into the High-Z state when RESET# is LOW. The target RESET# input includes a weak internal pull-up, if the target RESET# is left unconnected it will be pulled up to the HIGH state. NOTE Some compliant packages require the RESET# signal.
RSTO#	Target Output (Open Drain)	**Reset Output.** RSTO# is an open-drain output used to indicate when a Power On Reset (POR) is occurring within the target device and can be used as a system level reset signal. Upon completion of the internal POR the RSTO# signal will transition from low to high impedance after a user defined timeout period has elapsed. Upon transition to the high impedance state the external pull-up resistance will pull RSTO# HIGH.
INT#/ INT1#	Target Output / Controller Input (Open Drain)	**Interrupt**. When LOW, the target device is indicating that an internal event has occurred. This signal is intended to be used as a system level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output. When a second optional x8 IO target device exists within the same package, INT1# is used for device #1 and INT2# is used for device #2.

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Table 14 — xSPI Optional Signals (Informative) (cont'd)

Signal Name	Type	Description
ECS#/ ECS1#/ ECS2#	Target Output / Controller Input (Open Drain)	**Error Correction Status**. If ECC is enabled, the target device will drive the ECS# pin low if an on-chip ECC error has occurred. ECS# is an open-drain output. When a second optional x8 IO target device exists within the same package, ECS1# is used for device #1 and ECS2# is used for device #2.
WP#/ WP1#/ WP2#	Controller Output / Target Input	**Write Protect**. The WP pin controls the hardware locking feature of the device. The target WP# input includes a weak internal pull-up, if the target WP# is left unconnected it will be pulled up to the HIGH state. When a second optional x8 IO target device exists within the same package, WP1# is used for device #1 and WP2# is used for device #2.
V_{PP}	Power Supply	**Programming Power** when at a voltage above $V_{DD}Q$. NOTE Some target devices cannot withstand voltage above $V_{DD}Q$ on this signal connector.
RFU	Undefined	**Reserved for Future Use.** The package terminal may be connected to a circuit in the device. The function of the terminal is not currently defined or may be used for an optional signal available on some target devices. It is recommended to leave the terminal open and unconnected to external circuits or connected appropriately for the optional signal function.
NC	No Connection	**No Connection.** The package terminal has no connection to circuits in the device.
NU	Undefined	**No Use.** The package terminal must remain open and unconnected to external circuits.
NOTE The optional signals describe vendor-specific signal functions. Their behavior is outside the scope of this standard but is listed so their location within a package footprint is identified.		

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7.3 Fine-Pitch Ball Grid Array (FBGA) 24-Ball Footprint

This footprint has a 5 x 5 ball grid with 1 mm pitch between balls. The A1 ball position is not populated, to serve as an indication of footprint orientation, leaving a total of 24 balls. The ball grid is centered within the package body outline.

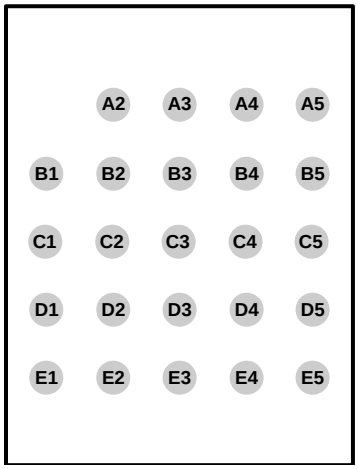

Figure 23 — FBGA 24-Ball Footprint

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7.3.1 Signal Assignments for 24-Ball FBGA Footprint

Table 15 — Signal Assignments for 24-Ball FBGA Footprint

Ball Location	xSPI Signal
A1	No Ball
A2	RFU / RSTO#
A3	RFU / CS2#
A4	RESET#
A5	RFU / INT# / ECS#
B1	RFU / CK#
B2	CK
B3	V_{SS}
B4	V_{DD}
B5	RFU
C1	$V_{SS}Q$
C2	CS# / CS1#
C3	DS/ DS1
C4	IO2
C5	RFU / VPP / WP#
D1	$V_{DD}Q$
D2	IO1
D3	IO0
D4	IO3
D5	IO4
E1	IO7
E2	IO6
E3	IO5
E4	$V_{DD}Q$
E5	$V_{SS}Q$

7.3.2 Package Physical Diagrams

Refer to JEDEC JEP95, MO-234 for physical package characteristics and drawings.

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7.4 0.5 mm-Pitch WLCSP (Wafer Level Chip Scale Package)

This footprint has ball grid with 0.5 mm pitch between balls. The number of balls depends on the size of the die. The ball grid is centered within the package body outline.

7.4.1 Ball Locations for a Minimally Sized Die

	1	2	3	4	5	6
A		RESET#	IO_7	V_{SS}	INT#	RFU (ECS#)
B	RFU (RSTO#)	V_{SSQ}	V_{DDQ}	CS#	V_{DD}	RFU (IO_8)
C	RFU (WP#)	IO_6	IO_3	IO_1	V_{SS}	RFU (IO_9)
D	RFU (CK#)	IO_5	CK	IO_2 / WP#	IO_4	RFU (IO_{10})
E	V_{DDQ}	DS	IO_0	V_{SSQ}	V_{PP}	RFU (IO_{11})
F	RFU (V_{SSQ})	RFU (V_{DDQ})	RFU (IO_{15})	RFU (IO_{14})	RFU (IO_{13})	RFU (IO_{12})

Balls A2:E5 – "Core" set of balls for Octal xSPI
Balls that are backward compatible to QSPI (Quad-SPI)
Additional optional balls for Octal xSPI implementations
Balls for future x16 variation

Figure 24— Ball Location Diagram (Top View – Balls Down)

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7.4.2 Ball Locations for a Large Die

	1	2	3	4	5	6	7	8	9	10
A		RFU		RFU		RFU		RFU		RFU
B	RFU		RFU		RFU		RFU		RFU	
C		RFU		RESET#	IO_7	V_{SS}	INT#	RFU (ECS#)		RFU
D	RFU		RFU (RSTO#)	V_{SSQ}	V_{DDQ}	CS#	V_{DD}	RFU (IO_8)	RFU	
E		RFU	RFU (WP#)	IO_6	IO_3	IO_1	V_{SS}	RFU (IO_9)		RFU
F	RFU		RFU (CK#)	IO_5	CK	IO_2 / WP#	IO_4	RFU (IO_{10})	RFU	
G		RFU	V_{DDQ}	DS	IO_0	V_{SSQ}	V_{PP}	RFU (IO_{11})		RFU
H	RFU		RFU (V_{SSQ})	RFU (V_{DDQ})	RFU (IO_{15})	RFU (IO_{14})	RFU (IO_{13})	RFU (IO_{12})	RFU	
J		RFU		RFU		RFU		RFU		RFU
K	RFU		RFU		RFU		RFU		RFU	RFU

Balls for future use

Figure 25 — Ball Location Diagram Large Die (Top View – Balls Down)

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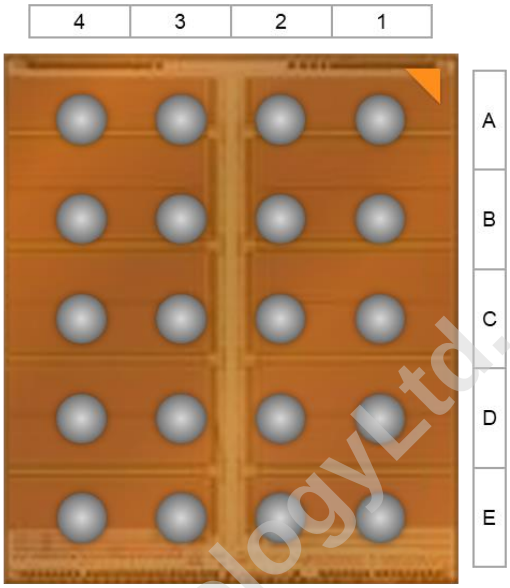
7.4.3 Example for Small Die with “Core” 4x5 Ball Matrix

	1	2	3	4
A	RESET#	IO_7	V_{SS}	INT#
B	V_{SSQ}	V_{DDQ}	CS#	V_{DD}
C	IO_6	IO_3	IO_1	V_{SS}
D	IO_5	CK	IO_2 / WP#	IO_4
E	DS	IO_0	V_{SSQ}	V_{PP}

Top View (Balls Down)



Bottom View (Balls Up)

NOTE It is recommended to use the RDL (redistribution layer) metal to create an orientation mark near the A1 ball.

Figure 26 — Example for Small Die with “Core” 4x5 Ball Matrix

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7.5 49-Ball BGA (Ball Grid Array) Package for Dual-Octal (x16 IO) xSPI

This footprint has ball grid with 1.0 mm pitch between balls. The ball matrix is a superset of the 24-ball FBGA layout and is backward compatible.

7.5.1 Ballout Descriptions

Table 16 — 49-Ball BGA Ballout Descriptions

	Count	Description	Required	Total
CS(n)#	1, 2	CS# (x16 chip) or CS1# (x8 chip-1) and CS2#* (x8 chip-2)	Yes	1 or 2
CK(n)	1, 2	CK (x16 chip) or CK1(x8 chip-1) and CK2* (x8 chip-2)	Yes	1 or 2
CK(n)#	1, 2	CK# (x16 chip) or CK1# (x8 chip-1) and CK2#* (x8 chip-2)	No	1 or 2
IO	16	IO[15:0] (x16 chip) or IO[7:0] (x8 chip-1) and IO[15:8] (x8 chip-2)	Yes	16
DS(n)	1, 2	DS (IO[15:0]) or DS1 (IO[7:0]) and DS2* (IO[15:8])	Yes	1 or 2
DS(n)#	1, 2	DS# (IO[15:0]) or DS1# (IO[7:0]) and DS2#* (IO[15:8])	No	1 or 2
RESET#	1	Hardware Reset	Yes	1
RFU/ ECS(n)#/ INT(n)#	1, 2	RFU/ Optional ECC Status/Internal Event: ECS#/ INT# (x16 chip) or ECS1#/ INT1# (Chip-1) and ECS2#*/ INT2#* (Chip-2)	No	1 or 2
V_{DD}	2	Power	Yes	2
$V_{DD}Q$	6	IO Power	Yes	6
V_{SS}	2	GND	Yes	2
$V_{SS}Q$	6	IO GND	Yes	6
RFU/ RDY#	1	RFU/ Optional Busy/Ready Status	No	1
RFU/ V_{PP}/ WP(n)#	1, 2	RFU/ Optional Write Protect: WP# (x16 chip) or WP1# (chip-1) and WP2#* (chip-2)	No	1 or 2
RFU/ RSTO#	1	RFU/ Optional Output indicating POR active	No	1
			Max Total	49

* These signals are only used in dual-die configurations.

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7.5.2 Signal Assignments for 49-Ball BGA Footprint

Table 17 — Signal Assignments for 49-Ball BGA Footprint

Ball Location	xSPI Signal
A1	RFU/ INT2#*/ ECS2#*
A2	RFU / WP2#*
A3	RFU/ RSTO#
A4	RFU/ CS2#*
A5	RESET#
A6	RFU/ INT1#/ ECS1#
A7	V_{SS}
B1	RFU / RDY#
B2	RFU/ CK#/ CK1#
B3	CK/ CK1
B4	V_{SS}
B5	V_{DD}
B6	RFU/ DS#/ DS1#
B7	$V_{SS}Q$
C1	V_{DD}
C2	$V_{SS}Q$
C3	CS#/ CS1#
C4	DS/ DS1
C5	IO2
C6	RFU/ V_{PP}/ WP1#
C7	$V_{DD}Q$
D1	$V_{SS}Q$
D2	$V_{DD}Q$
D3	IO1
D4	IO0
D5	IO3
D6	IO4
D7	CK2#*

Ball Location	xSPI Signal
E1	$V_{DD}Q$
E2	IO7
E3	IO6
E4	IO5
E5	$V_{DD}Q$
E6	$V_{SS}Q$
E7	CK2*
F1	IO9
F2	IO11
F3	$V_{DD}Q$
F4	DS2*
F5	IO8
F6	$V_{DD}Q$
F7	IO10
G1	IO13
G2	IO15
G3	$V_{SS}Q$
G4	DS2#*
G5	IO12
G6	$V_{SS}Q$
G7	IO14

* These balls are only used in dual-die configurations that do not share a common Chip Select (CS#) ball; in configurations that do share a common CS# ball, these balls should then be RFU.

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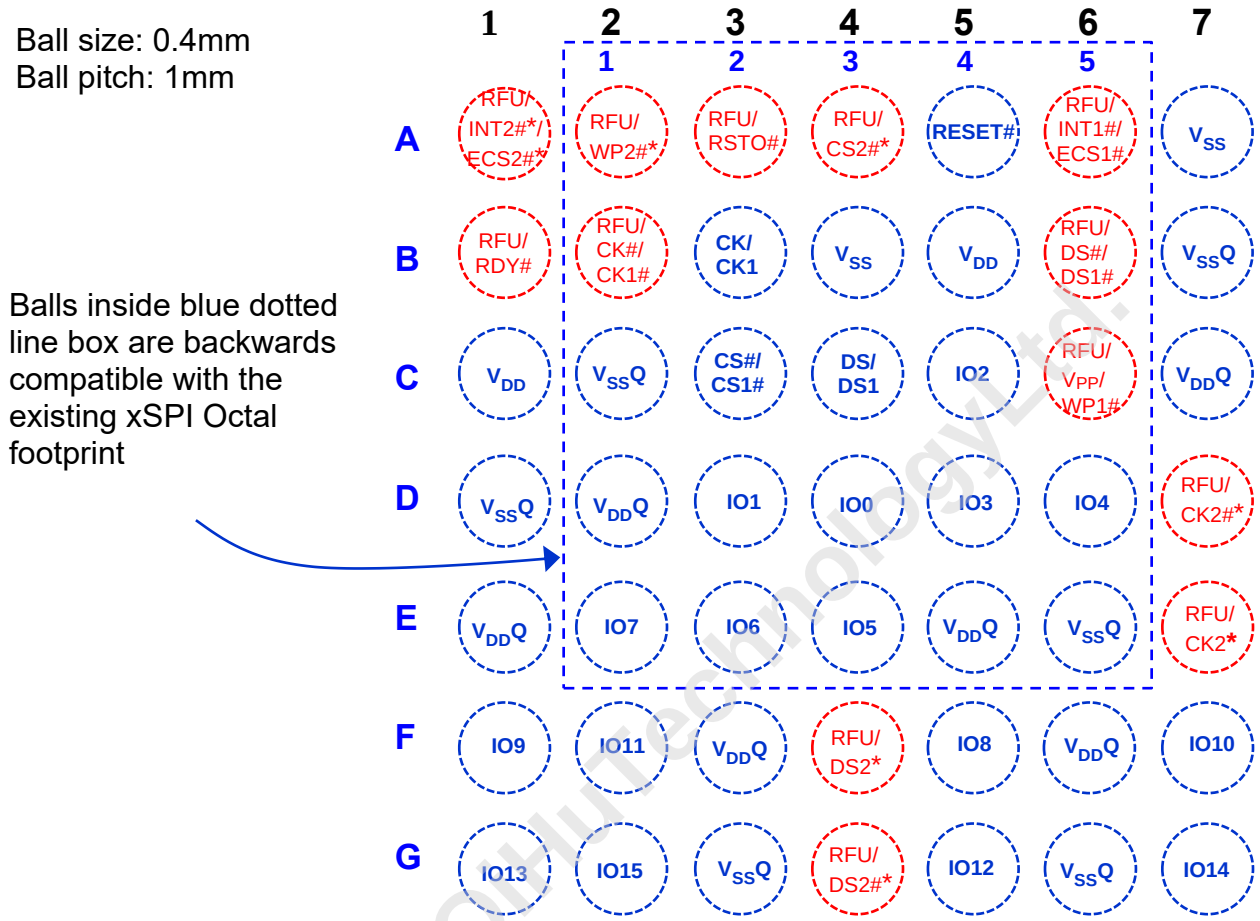
7.5.3 49-Ball BGA Package Layout



* = These balls are only used in dual-die configurations that do not share a common Chip Select (CS#) ball; in configurations that do share a common CS# ball, these balls should then be RFU.

Color Legend: Blue = Mandatory signals and PCB ball landing pads
Red = Optional signals, but required PCB ball landing pads

Figure 27 — 49-Ball BGA Ball Location Diagram (Top View – Balls Down)

7.5.4 Package Physical Diagrams

Refer to JEDEC JEP95, MO-331-P8.00x8.00-10045-49D for physical package characteristics and drawings.

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8 xSPI Electrical

8.1 Introduction

This chapter defines electrical specifications for the xSPI based on the JEDEC JESD84-B51 HS400 mode standard. The interface can operate in one of four speed grades:

- xSPI-200: up to 100 MHz, up to 200 MT/s
- xSPI-266: up to 133 MHz, up to 266 MT/s
- xSPI-333: up to 166 MHz, up to 333 MT/s
- xSPI-400: up to 200 MHz, up to 400 MT/s

8.2 xSPI Signals

The xSPI has the following signals:

- CK: The clock line is an output of the controller and an input of the target device. The CK driver operates in push-pull mode.
  - CK#: The clock complement signal is optional and used when a target device requires differential clock and is considered as part of the controller to target clock when used.
- CS#: Unidirectional output of the controller and an input of the target device, active LOW chip select signal.
- IO[7:0]: Bidirectional data signals. Controller and Target drivers are operating in push-pull mode.
- DS: Data Strobe. This signal is an input to the controller during read data transfers and is driven by the target. In some cases DS is bi-directional and may be driven by the controller during the command and command modifier phases or during write data transfers.

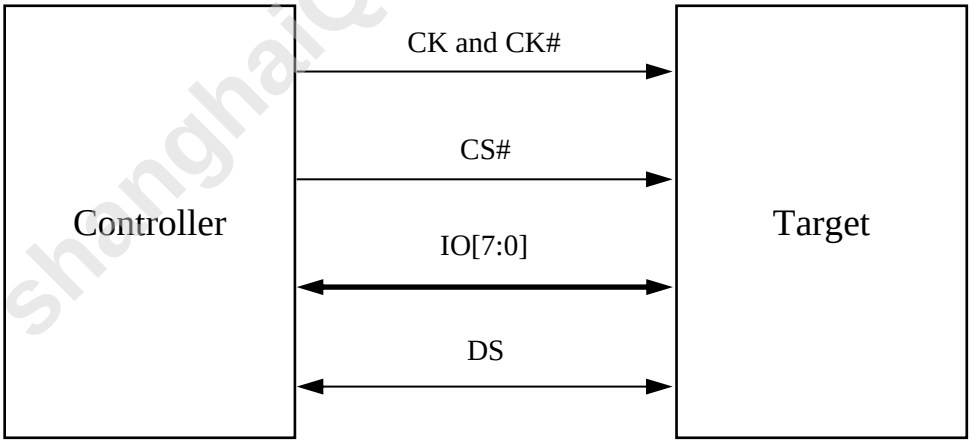

Figure 28 — xSPI Controller-Target Connections

For high frequency DDR operation, it is expected that the host will use a programmable delay element on its DS input for sampling the data at the optimal point. It is highly recommended for the device to have means to support calibration of that delay. A delay element may also be used by the host for positioning CK optimally relative to the data. It is recommended that the device will have means to support calibration of this delay too.

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8.3 Power Supply

In the xSPI, V_{DD} is used as the target device internal functions power supply. V_{DDQ} is the interface power supply.

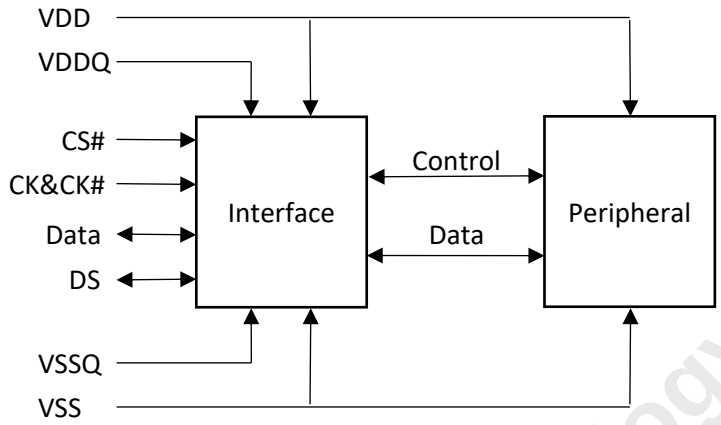

Figure 29 — xSPI Target Internal Power Diagram

8.4 Bus Capacitance and Programmable Output Driver Strength

The bus capacitance on each line of the xSPI bus is the sum of the bus controller capacitance, the bus capacitance itself, and the capacitance of each target device. The sum of controller and bus capacitance is fixed for one application but may vary between different applications. The total bus capacitance on each line may vary in one application with the number of the inserted target devices.

NOTE This standard covers xSPI bus systems with up to 12 pF bus capacitance on each line. Future updates to the standard may cover systems with higher bus capacitance.

Programmable output driver strength (type) provides flexibility to adjust the driver output impedance to compensate for variation in bus capacitance, to meet the required AC timing characteristics of an xSPI speed grade.

8.4.1 Device Capacitance

Each controller or target connected to the xSPI bus should not exceed the single device capacitance maximum.

Table 18 — Device Capacitance

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Single Device Capacitance	CDEVICE			6	pF	

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8.4.2 xSPI Reference Load

The circuit below shows the reference load used to define the xSPI controller and target device output timings, overshoot and undershoot parameters. The reference load is made up by the transmission line and the $C_{REFERENCE}$ capacitance.

The reference load is not intended to be a precise representation of any specific system environment. System designers should use IBIS or other simulation tools to correlate the reference load to the system environment. Manufacturers should correlate to their production test conditions.

Delay time (Td) of the transmission line has been introduced to make the reference load independent of the PCB technology and trace length.

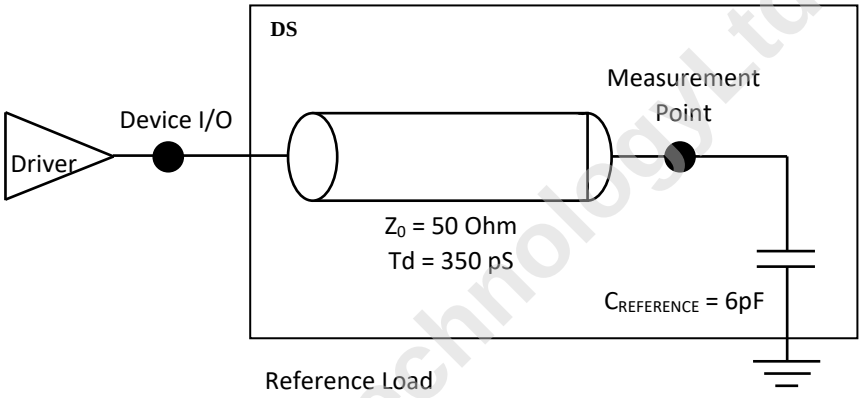

Figure 30 — xSPI Reference Load for 200 MHz DDR Operation

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8.4.3 Driver Types Definition

Driver Type-0 is defined as mandatory for the xSPI device while four additional driver types (1, 2, 3, and 4) are defined as optional to allow support for wider range of capacitive loads. The host may select the most appropriate driver type of the device (if supported) to achieve optimal signal integrity performance. Note that the driver strength definitions are the same for the 3 V, 1.8 V, and 1.2 V $V_{DD}Q$.

Driver Type-0 is targeted for transmission-line based distributed systems with 50 Ω nominal line impedance. Therefore, it is defined as a 50 Ω nominal driver.

For xSPI, when tested with the reference load defined in the previous clause, Driver Type-0 or Driver Type-1 or Driver Type-4 shall meet all AC characteristics and xSPI device output timing requirements. The four optional driver types are defined with respect to Driver Type-0. Table 19 summarizes the nominal impedance characteristics for the five driver types.

Table 19 — I/O Driver Strength Types

Driver Type Value	Support	Nominal Impedance	Approximated Driving Capability Compared to Type-0	Comments
0	Mandatory	50 Ω	x1	Default driver type. Supports up to 200 MHz operation when driving the reference load.
1	Optional	33 Ω	x1.5	
2	Optional	66 Ω	X0.75	
3	Optional	100 Ω	X0.5	For low noise and low EMI systems. Maximal operating frequency is determined by the system design.
4	Optional	40 Ω	x1.2	
NOTE 1 Support of Driver Type-0 is mandatory. NOTE 2 Nominal impedance is defined by I-V characteristics of the output driver at 0.5 x $V_{DD}Q$. NOTE 3 Variance in the Nominal Impedance can be up to +/- 20%.				

If the controller or target devices support the optional driver types, the host may use them to optimize the signal integrity in the system. To do so, the host designer may simulate its specific system using device driver models. The host can select the optimal driver type that may drive the host system load at the desired operating frequency with minimal noise generated.

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8.4.3.1 Driver Type Selection

The xSPI target device output driver strength may be configured by writing to a register as indicated in SFDP. The controller drivers can also be configured in a similar fashion. The definition of the method for configuring the controller bus drivers is beyond the scope of this standard.

Figures 31 and 32 show the IO circuitry for each of the signals. Dotted lines indicate optional elements.

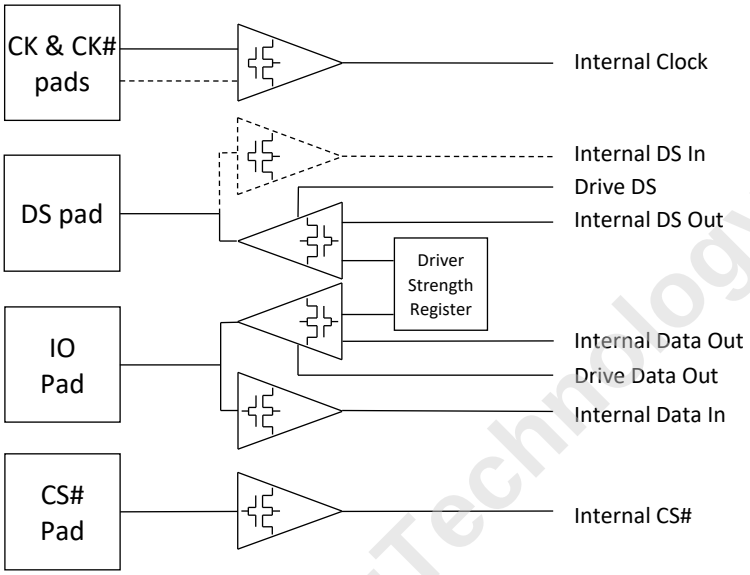

Figure 31 — Target I/O

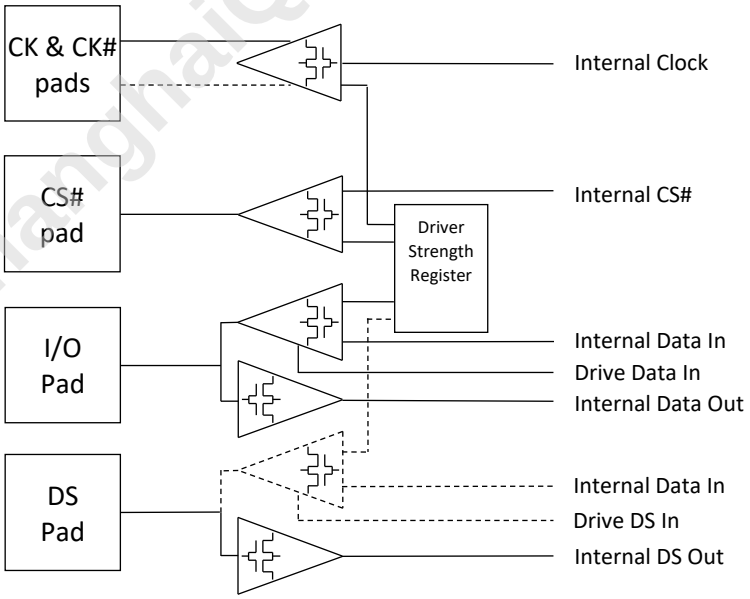

Figure 32 — Controller I/O

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8.5 xSPI Input and Output Voltage Levels

The device input and output voltages must be within one of the following I/O power supply ($V_{DD}Q$) voltage ranges. The voltage parameters for each of the voltage ranges are defined in JESD8-26 (1.2 V) and JESD8-31 (1.8 V).

8.6 Leakage Current

The device minimum and maximum leakage currents are specified in Table 20 and Table 21.

8.6.1 Leakage Current at 1.2 V and 1.8 V

Table 20 — Leakage Current at 1.2 V and 1.8 V

Parameter	Min	Max	Voltage
Input leakage current	-5	5	µA
Output leakage current	-5	5	µA

8.6.2 Leakage Current at 3 V

Table 21 — Leakage Current at 3 V

Parameter	Min	Max	Voltage
Input leakage current	-10	10	µA
Output leakage current	-10	10	µA

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8.7 AC Timing Specifications

8.7.1 Controller Output to Target Input Timing

Figure 33 shows the bus input timing for the xSPI target device.

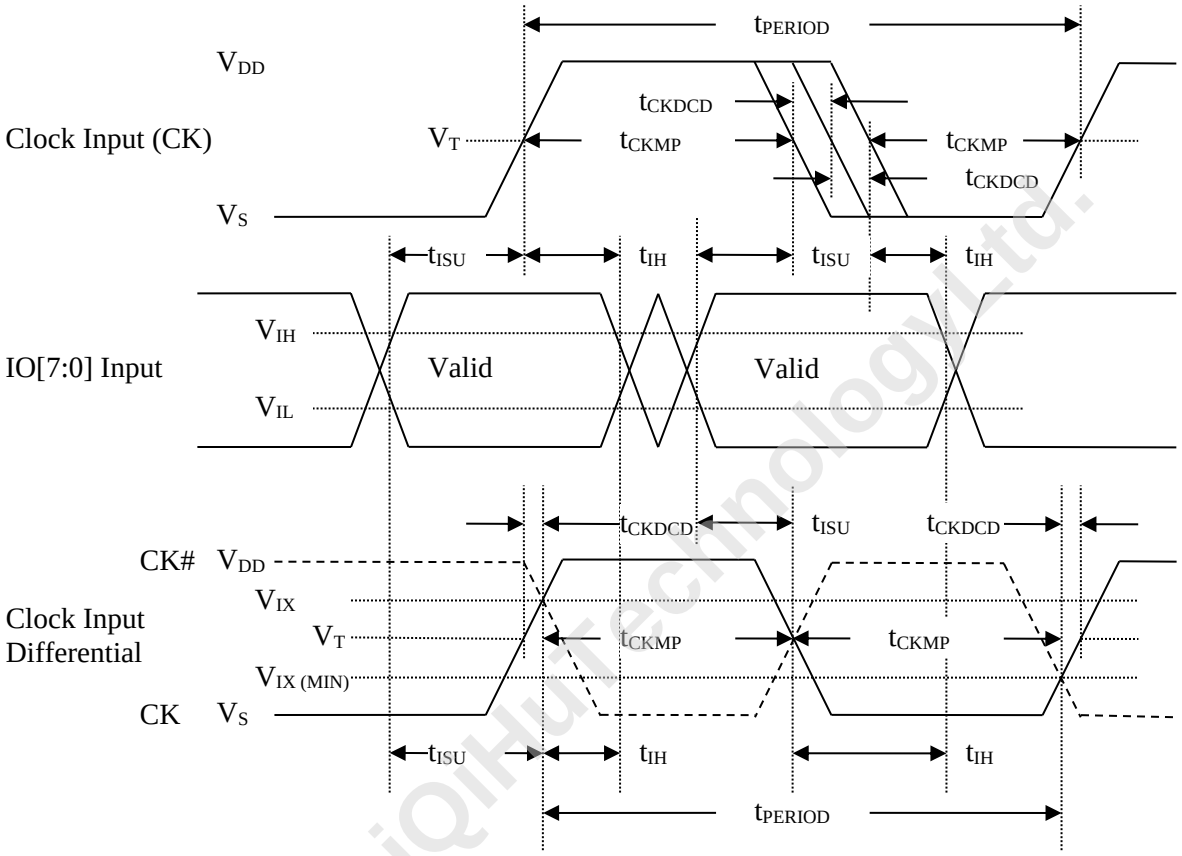

Figure 33 — xSPI Target Data Input Timing

Table 22 — Clock Input Threshold Levels

Parameter	Symbol	Min	Max	Unit
Clock Input Threshold (AC)	$V_{T(AC)}$	0.50 • V_{DD}	0.50 • V_{DD}	V
Input Differential Crossing (AC)	$V_{IX(AC)}$	0.4 • V_{DD}	0.60 • V_{DD}	V

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8.7.1 Controller Output to Target Input Timing (cont'd)

Table 23 — xSPI Device Input Timing

Parameter	Symbol	xSPI400		xSPI333		xSPI266		xSPI200		Unit	Comments
		Min	Max	Min	Max	Min	Max	Min	Max		
Input CK											
Cycle Time Data Transfer Mode	t_{PERIOD}	5		6		7.5		10		ns	200 MHz (max) between the rising edges with respect to V_T.
Slew Rate	SR	1.125		0.94		0.75		0.56		V/ns	With respect to V_{IH}/V_{IL}.
Duty Cycle Distortion	t_{CKDCD}	0.0	0.25	0.0	0.3	0.0	0.375	0.0	0.5	ns	Allowable deviation from an ideal 50% duty cycle with respect to V_T. Includes jitter and phase noise.
Minimum Pulse Width	t_{CKMPW}	2.25		2.7		3.375		4.5		ns	With respect to V_T.
Input Signals (Referenced to CK)											
Input Setup Time	t_{ISUddr}	0.5		0.6		0.8		1.0		ns	With respect to V_{IH}/V_{IL}.
Input Hold Time	t_{IHddr}	0.5		0.6		0.8		1.0		ns	With respect to V_{IH}/V_{IL}.
Slew Rate @ 1.2 V	SR	0.75		0.62		0.50		0.38		V/ns	With respect to V_{IH}/V_{IL} and xSPI reference load.
Slew Rate @ 1.8 V	SR	1.125		0.94		0.75		0.56		V/ns	With respect to V_{IH}/V_{IL} and xSPI reference load.
Slew Rate @ 3.0 V	SR	2.06		1.72		1.37		1.03		V/ns	With respect to V_{IH}/V_{IL} and xSPI reference load.

8.7.2 Target Output to Controller Input Timing

Figure 34 shows the bus output timing for the xSPI target device.

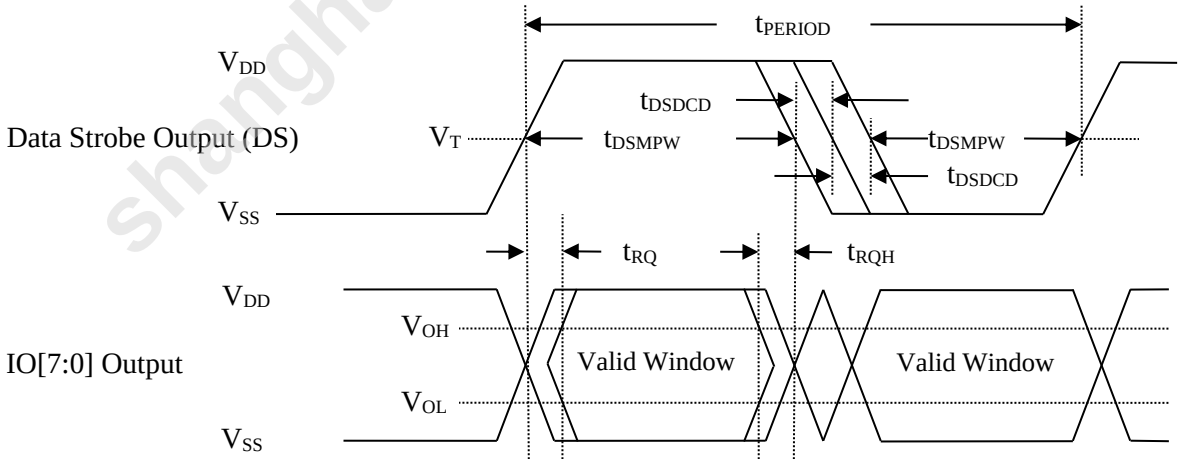

Figure 34 — xSPI Target Data Output Timing

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8.7.2 Target Output to Controller Input Timing (cont'd)

Table 24 — xSPI Device Output Timing

Parameter	Symbol	xSPI400		xSPI333		xSPI266		xSPI200		Unit	Comments
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Strobe											
Cycle Time Data Transfer Mode	t_{PERIOD}	5		6		7.5		10		ns	200 MHz (max) between the rising edges with respect to V_T.
Duty Cycle Distortion	t_{DSDCD}	0.0	0.2	0.0	0.24	0.0	0.3	0.0	0.4	ns	Allowable deviation from the input clock duty cycle distortion (t_{CKDCD}) with respect to V_T. Includes jitter and phase noise.
Minimum Pulse Width	t_{DSMPW}	2.05		2.46		3.075		4.1		ns	Minimum Pulse Width of DS is smaller than that of CK since the target is allowed to add distortion when generating DS from CK. With respect to V_T.
Output DATA (Referenced to DS)											
Output skew	t_{RQ}		0.4		0.48		0.6		0.8	ns	With respect to V_{OH}/V_{OL} and xSPI reference load.
Output hold skew	t_{RQH}		0.4		0.48		0.6		0.8	ns	With respect to V_{OH}/V_{OL} and xSPI reference load.

NOTE Controller CK edges are the trigger for target IO and DS edges. IO and DS edges therefore always follow their related (triggering) CK edges.

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8.7.3 xSPI CK and DS to CS# Signal Timing

Figure 35 and Figure 36 show the timing relationship between the CS#, CK, and DS signals.

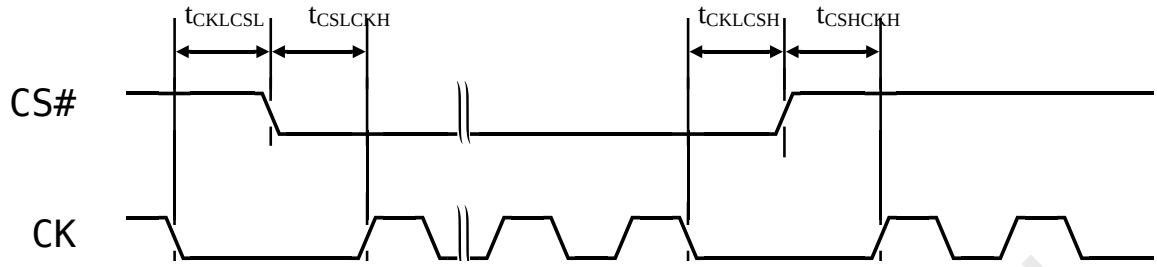
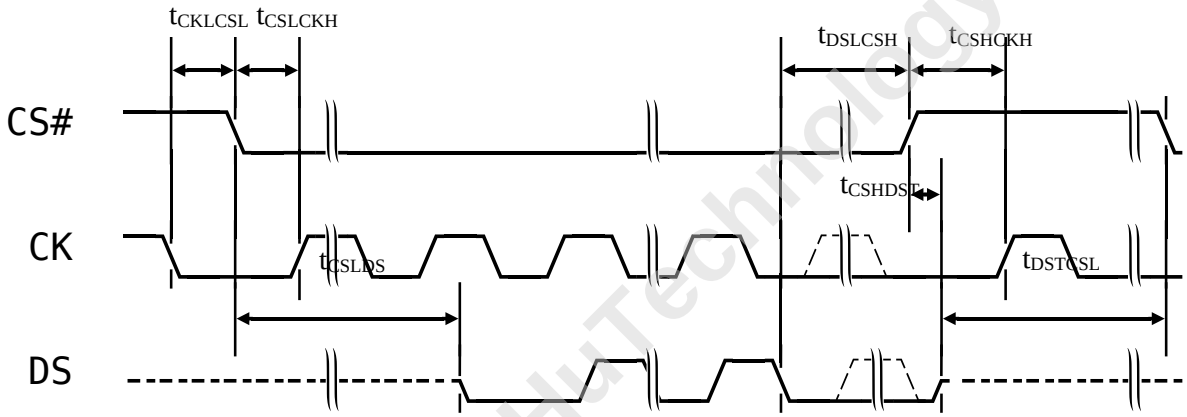


Figure 35 — CK to CS# Signal Timing



NOTE The controller needs to count valid DS edges. After receiving the required number of data bytes, the controller will de-assert CS#. By that time there may be one or more “dummy” edges which could cause one or more “dummy” DS edges.

NOTE CK must be gated to meet the spec in this diagram.

Figure 36 — DS to CS# Signal Timing

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8.7.3 xSPI CK and DS to CS# Signal Timing (cont'd)

Table 25 — Relative Timing of the CS#, DS, and CK Signals

Parameter	Symbol	xSPI400		xSPI333		xSPI266		xSPI200		Unit	Comments
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock LOW to CS LOW	t_{CKLCSL}	4		4.8		6		8		ns	
CS LOW to Clock HIGH	t_{CSLCKH}	4		4.8		6		8		ns	
Clock LOW to CS HIGH	t_{CKLCSH}	4		4.8		6		8		ns	
CS HIGH to Clock HIGH	t_{CSHCKH}	4		4.8		6		8		ns	
DS LOW to CS HIGH	t_{DSLCSH}	80% of t_{PERIOD}		80% of t_{PERIOD}		80% of t_{PERIOD}		80% of t_{PERIOD}			
CS HIGH to DS Tri-State	t_{CSHDST}	0	t_{PERIOD}	0	t_{PERIOD}	0	t_{PERIOD}	0	t_{PERIOD}	ns	
CS LOW to DS LOW	t_{CSLDSL}	0		0		0		0		ns	
DS Tri-State to CS LOW	t_{DSTCSL}	0		0		0		0		ns	

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Annex A - (Informative) Differences Between Revisions

This annex briefly describes most of the changes made to entries that appear in this standard, JESD251C, compared to its predecessor, JESD251B (September 2021), JESD251A (February 2020), and JESD251 (July, 2018). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

A.1 Differences between JESD251C and JESD251B

Clause	Description of change
NEW	Updated Table of Contents to include list of Tables and Figures
8.7.2	Elimination of output minimum slew rates (from item 1775.74)

A.2 Differences between JESD251B and JESD251A

Updated Table of Contents

Globally changed:

1) "Master" to "Controller"
2) "master" to "controller"
3) "Slave" to "Target"
4) "slave" to "target"

Clause	Description of change
NEW	Added new 7.5, 7.5.1, 7.5.2, 7.5.3, and 7.5.4 for 1.0 mm pitch 49-ball BGA (From item 1775.64, JC-42.4-20-243)
8	Renumbered tables and figures to accommodate those previously inserted in 7.4 and newly inserted in 7.5

A.3 Differences between JESD251A and JESD251

Clause	Description of change
2	Added reference for JESD8-xx (3 V High-Speed LVCMOS), and JESD252.
7.2	Table 14, added signal: IO[15:8]
7.4	Renumbered to 7.3.1
7.5	Renumbered to 7.3.2
NEW	Added new 7.4, 7.4.1, 7.4.2, and 7.4.3 for 0.5 mm pitch WLCSP (From item 1775.59, JC-42.4-19-402)

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Standard Improvement Form **JEDEC Standard JESD251C**

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

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3. Other suggestions for document improvement:

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