JEDEC STANDARD

Addendum No. 1 to JESD251, Optional x4 Quad I/O With Data Strobe

JESD251-1.01

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Addendum No. 1 to JESD251, OPTIONAL x4 QUAD I/O WITH DATA STROBE

Contents

Figures

Tables

Foreword

This document was prepared by the JC42.4_3 Serial Flash task group authorized by the JC-42.4 Non-Volatile Memory subcommittee.

This standard is intended for use by SoC, ASIC, ASSP, and FPGA developers or vendors interested in incorporating a initiator (sometimes called 'controller') interface having a low signal count and high data transfer bandwidth with access to multiple sources of target devices compliant with the interface. It is also, intended for use by peripheral developers or vendors interested in providing target devices compliant with the standard, including non-volatile memories, volatile memories, graphics peripherals, networking peripherals, FPGAs, sensors, etc.

Introduction

This purpose of the addendum is to add an optional 4-bit bus width (x4) to JESD251, xSPI standard. The xSPI interface currently supports a x1 interface that acts as a bridge to legacy SPI functionality as well as the x8 interface intended to achieve dramatically higher bus performance than legacy SPI memory implementations.

Legacy x4 SPI devices are currently available that support DDR operation at 100MHz which achieves a 100MB/s bus throughput. This 100MB/s data rate is about as high as the legacy quad SPI interface can achieve without adopting additional infrastructure.

The xSPI standard describes two infrastructure mechanisms that are intended to achieve higher bus throughput. First, the bus width is increased from four to eight bits. Second, a data strobe has been added to assist in host data capture. The expansion to eight bits and the addition of a data strobe doubles the bus throughput and allows the xSPI interface to achieve a 400MB/s data rate.

The gap between the legacy 100MB/s throughput and the new xSPI throughput of 400MB/s is substantial. The addendum adds a single data strobe pin to double the throughput (200MB/s).

The addendum is intended to fit within the scope of the JEDEC JESD251, xSPI standard as an optional feature. The standard specifies x1, x4 and x8 behavior. Bus width options offered by manufacturers would include: **x1/x8 (JEDEC xSPI)**, **x1/x4/x8** or **x1/x4**. Pinout of the x4 device is identical to the existing xSPI standard with the exception that the upper four bits of the I/O bus are unpopulated or unused. Besides having four fewer I/O pins, there are two other important differences between the existing x8 option and the x4 option:

1. The x4 option uses a single 8-bit byte for the Command whereas the x8 option requires two 8-bit bytes (Word) for the Command.
2. The x4 option uses a slightly different command protocol: The x8 option uses DDR mode for Commands, Address, and Data while the x4 option uses SDR mode for Commands and DDR mode for Address and Data.

Addendum No. 1 to JESD251, OPTIONAL x4 QUAD I/O WITH DATA STROBE

(From JEDEC Board Ballot JCB-18-34, formulated under the cognizance of the JC-42.4 Committee on Non Volatile Memory.)

1 Scope

The JESD251 document defines the SPI (1-1-1) and Octal (8-8-8) I/O modes, including features, functionalities, package, and ball/signal assignments with the exception of what is stated within this addendum.

2 x4 Key Features

The following is a summary of the x4 Quad I/O features:

2.1 General Features

- Speed grades with data transfer rates up to
  - 200MT/s (200MHz Clock)
  - 167MT/s (167MHz Clock)
  - 133MT/s (133MHz Clock)
  - 100MT/s (100MHz Clock)

2.2 Topology

- Single initiator, multiple targets, per interface port
  - One chip select per target,
  - Fits existing x8 footprint with the exception that I/O[7:4] would be unused,
  - The major infrastructure addition to the legacy SPI interface is a Data Strobe,
  - Manufacturers would have the option to include x4 functionality on their x8 product offerings or to eliminate the x8 functionality on their x4 product offerings.

2.3 x4 Interface Features

- Input/Output Power Supplies Options:
  - 1.2V, 1.8V, or 3V
- Signal Count Options:
  - Seven-signal target interface (Clock, CS#, 4-bit Data Bus, Data Strobe),
  - Eight-signal target interface (Differential Clock, CS#, 4-bit Data Bus, Data Strobe),
  - Interface may operate in 1S-1S-1S I/O mode without data strobe at ≤ 50MHz SDR.
- I/O Protocol Modes:
  - Transaction phases = Command-Modifier-Data,
  - Transfer bit width options in each phase = W = 1, or 4,
  - Data rate options in each phase = R = S for SDR or D for DDR,
  - 1S-1S-1S (24-bit addressing) for power-up and configuration,
  - 4S-4D-4D (32-bit addressing in Profile 1.0).
- Target Reset Options:
  - Power-on Reset (POR) – mandatory,
  - In-band Reset (JESD252) – mandatory,
  - Separate Reset Signal – optional.
- Power management option:
  - Deep Power Down (DPD) enter and exit commands.

2.4 Protocol Modes defined for the xSPI interface

- 1S-1S-1S (defined in JESD251, 5.4)
  - One I/O signal used during command transfer, command modifier transfer, and data transfer. All phases are SDR.
- 8D-8D-8D (defined in JESD251, 5.4)
  - Eight I/O signals used during command transfer, command modifier transfer, and data transfer. All phases are DDR.
- 4S-4D-4D
  - Four I/O signals used during command transfer, command modifier transfer, and data transfer. The command transfer is done in SDR mode while command modifier transfer, and data transfer are always using DDR
- A target device must implement the 1S-1S-1S protocol mode and either the 4S-4D-4D or 8D-8D-8D protocol mode. A target device may optionally implement all three protocol modes.
- The 1S-1S-1S mode is the preferred default protocol following Power-On-Reset (POR) but, target devices may be configured to reset into the octal mode. Target devices may implement other modes of operation. The supported modes are indicated in the SFDP.
- For example, 4S-4D-4D or 8D-8D-8D mode can be made the default mode if so desired. The initiator must determine the default protocol mode of each target after POR. This may be done through prior knowledge of the system design. The initiator may later reconfigure a target to use other target supported modes. In some devices switching between modes is done through issuing a command or a series of commands while in other devices that change is done through a modification of bits in control registers. The modes supported by a target and the method for switching between modes are indicated in the SFDP.

3 xSPI Overview

3.1 xSPI Performance Enhancements (see JESD251, 5.1)

3.2 xSPI Topology and Signal Descriptions (see JESD251, 5.2)

3.3 xSPI Signal Protocols

During the time that CS# is active (LOW) the clock signal (CK) is toggled while command information is first transferred on the data (I/O) signals from the initiator to the target. The clock continues to toggle during any period required for information access in the target. The clock continues to toggle during the transfer of read data from the target to the initiator or write data from the initiator to the target. When the initiator has transferred the desired amount of data, the initiator drives the CS# inactive (HIGH). The period during which CS# is active is called a transaction on the bus.

While CS# is inactive, the CK is not required to toggle. CK may stop toggling when LOW as a means of lowering power consumption or inserting delay within a transaction for flow control by the initiator. CK must always complete at least one rising edge and one falling edge before stopping at LOW. This requirement for a minimum of one rising and falling edge in turn requires that DDR transfers always occur in two transfer increments e.g. two bytes (word) for 8-bit wide transfers. SDR transfers must occur in one byte increments. Some target devices may have limitations on the maximum time that CK may stop (remain LOW) or, on the maximum time CK may be HIGH (i.e. a minimum clock frequency during a transaction); these are target device specific system design consideration.

There are up to four phases of activity within each transaction:

- Command transfer from initiator to target;
- Command Modifier transfer from initiator to target;
- Initial Access Latency (also used for I/O signal direction turn around in a read transaction);
- Data transfer (target to initiator in a read transaction or initiator to target in a write transaction

The command transfer occurs at the beginning of every transaction. The command modifier, initial access latency, and data transfer phases are optional and their presence depends on the protocol mode or command transferred.

The number of parallel I/O signals used during the command modifier and data phases depends on the current protocol mode or command transferred. The initial access latency phase does not use the I/O signals for information transfer. The protocol mode options are described by the data rate and the I/O width (number of I/O signals) used during the command, command modifier, and data phases in the following format:

3.3 xSPI Signal Protocols (cont'd)

WR-WR-WR where:

- The first WR is the command bit width and rate
- The second WR is the command modifier bit width and rate
- The third WR is the data bit width and rate.

The bit width value may be 1, 4, or 8. R has a value of S for SDR, or D for DDR. SDR has the same transfer value during the rising and falling edge of a clock cycle. DDR may have different transfer values during the rising and falling edges of each clock.

Examples:

- 1S-1S-1S means that the command is 1 bit wide SDR, the command modifier is 1 bit wide SDR, and the data is one bit wide SDR.
- 4S-4D-4D means that the command is 4 bits wide SDR, and the command modifier, and data transfers are always 4 bits wide DDR.
- 8D-8D-8D means that the command, command modifier, and data transfers are always 8 bits wide DDR.

Protocol Modes defined for the xSPI interface:

- 1S-1S-1S
  - One I/O signal used during command transfer, command modifier transfer, and data transfer. All phases are SDR.
- 4S-4D-4D
  - Four I/O signals used during command transfer, command modifier transfer, and data transfer. Command phase is SDR and the other phases are DDR.
- 8D-8D-8D
  - Eight I/O signals used during command transfer, command modifier transfer, and data transfer. All phases are DDR.

A target device must implement the 1S-1S-1S protocol mode and either the 4S-4D-4D or 8D-8D-8D protocol mode. A target device may optionally implement all three protocol modes.

The 1S-1S-1S mode is the preferred default protocol following Power-On-Reset (POR) but, target devices may be configured to reset into the Quad or Octal mode. Target devices may implement other modes of operation. The supported modes are indicated in the SFDP.

For example, 4S-4D-4D mode can be made the default mode if so desired. The initiator must determine the default protocol mode of each target after POR. This may be done through prior knowledge of the system design. The initiator may later reconfigure a target to use other target supported modes. In some devices switching between modes is done through issuing a command or a series of commands while in other devices that change is done through a modification of bits in control registers. The modes supported by a target and the method for switching between modes are indicated in the SFDP.

3.3 xSPI Signal Protocols (cont'd)

A protocol mode phase using four I/O signals uses I/O[3:0]. The LSb of each byte is placed on I/O[0] with each higher order bit on the successively higher numbered I/O signals. Sequential data bytes in DDR are transferred in lowest address to highest address order.

The bitmapping during bus transactions follows the legacy SDR mode of presenting the Command and shifts to a DDR mode to identify the target address and send/receive data.

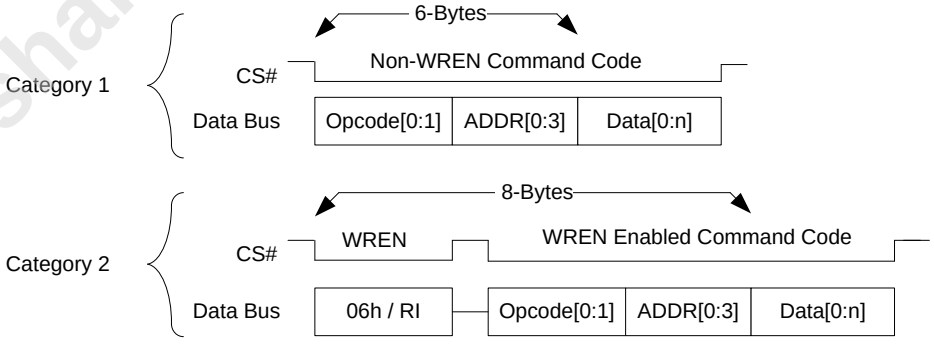
Table 1 — 4S-4D-4D Bit Positions

I/O	Command Bits		Command Modifier Bits (address)					Latency	Data Byte 0		Data Byte 1	
0	4	0	28	24	…	4	0	X …	4	0	4	0
1	5	1	29	25	…	5	1	X …	5	1	5	1
2	6	2	30	26	…	6	2	X …	6	2	6	2
3	7	3	31	27	…	7	3	X …	7	3	7	3
4	X	X	X	X	X…	X	X	X …	X	X	X	X
5	X	X	X	X	X…	X	X	X …	X	X	X	X
6	X	X	X	X	X…	X	X	X …	X	X	X	X
7	X	X	X	X	X…	X	X	X …	X	X	X	X

4 Profile 1.0 4S-4D-4D Commands

Commands are grouped into two Categories as follows:

1. Category 1: Non-WREN Enabled Commands require a single CS# cycle.
2. Category 2: WREN Enabled Commands must be prefixed by one additional CS# cycle for a write enable (WREN) command.



4 Profile 1.0 4S-4D-4D Commands (cont'd)

Table 2 — Profile 1.0 commands used in 4S-4D-4D protocol mode (required commands)

Command Function	Command Code (Hex)	Category	Additional Modifier Bytes	Initial Latency (CK cycles)	Data Bytes	Transaction Format	Req. Max. Freq. (MHz)
Read Fast	0B / EE / SFDP	1	4	1+	2+	1.B	
Write Enable (WREN)	06	1	0	0	0	1.A	
Write Disable	04	1	0	0	0	1.A	
Program	02 / 12 / SFDP	2	4	0	2+	1.D	
Erase 64+Kbytes	D8 / DC / SFDP	2	4	0	0	1.C	
Program / Erase Suspend	B0 / 75 / SFDP	1	0	0	0	1.A	
Program / Erase Resume	30 / 7A / D0 / SFDP	1	0	0	0	1.A	
Read Status Register	05	1	0/4/SFDP	4/8/SFDP	1	1.B	

4 Profile 1.0 4S-4D-4D Commands (cont'd)

Table 3 — Profile 1.0 commands used in 4S-4D-4D protocol mode (optional commands)

Command Function	Command Code (Hex)	Category	Additional Modifier Bytes	Initial Latency (CK cycles)	Data Bytes	Transaction Format	Req. Max. Freq. (MHz)
Read SFDP 4S-4D-4D	5A	1	3/4	8/20	2+	1.B	50+
Read Fast Wrapped	0C/SFDP	1	4	1+	2+	1.B	
Setup Read Wrap	C0	1	4	0	2+	1.D	
Erase 4Kbytes	20/21/SFDP	2	4	0	0	1.C	
Erase 32Kbytes	52/53/SFDP	2	4	0	0	1.C	
Erase Chip	C7	2	0	0	0	1.A	
Read Configuration Register	15	1	4	4	1	1.B	
Read Flag Status Register	70	1	0	8	1	1.A	
Read Register	65	1	1/4/SFDP	1+	1+	1.B	
Read Volatile Register	85/71/SFDP	1	4	4/8/SFDP	1	1.B	
Read NV Register	B5/15/65/SFDP	1	4	4/8/SFDP	1	1.B	
Write Status-Configuration Register	01	2	0/4/SFDP	0	1+	1.D	
Clear Flag Status Register	50	1	0	0	0	1.A	
Write Register	71/SFDP	2	1/4/SFDP	0	1/2	1.D	
Write Volatile Register	81/72/71/SFDP	2	4	0	1	1.D	
Write NV Register	B1/01/71/SFDP	2	4	0	1	1.D	
Enter Deep Power Down	B9	1	0	0	0	1.A	
Exit Deep Power Down	AB	1	0	0	0	1.A	
Soft Reset	F0	1	1	0	0	1.B	
Reset Enable	66	1	0	0	0	1.A	
Soft Reset and Enter default protocol mode	99	1	0	0	0	1.A	
Enter default protocol mode	FF	1	0	0	0	1.A	

NOTE 1 New device designs should assign Command Codes from Table 2 and Table 3 for commands that are specified in the table rather than pick other codes.

NOTE 2 It is recommended that new device designs should only pick Command Codes that are not mentioned in Table 2 and Table 3 for new commands.

NOTE 3 The size of block erased by the Erase 64+Kbytes and Erase 64+Kbytes4 command is indicated in the SFDP.

NOTE 4 Some commands have multiple recommended code value options that are device specific. New device designs should pick one of the recommended code values. The device supported command codes are indicated in the SFDP. This is indicated in the table by listing SFDP as one of the command code options.

NOTE 5 Some commands have multiple recommended command modifier length options that are device or device configuration specific. New device designs should pick one of the recommended command modifier length. The target device supported command modifier length options and any configuration methods are indicated in the SFDP.

5 Profile 1.0 4S-4D-4D Transaction Formats

Several commands use either a 3 or 4 byte address depending on a configuration setting of the target device. Several commands have a variable initial access latency that depends on a configuration setting of the target device. The length of data transfer depends on the command or operating conditions. The initiator must be aware of these configuration settings and command behaviors in order to select the correct command format.

The following transaction formats are used in Profile 1.0 mode 4S-4D-4D:

- Format 3.A: Command Only
- Format 3.B: Command and Read Data
- Format 3.C: Command, 3-byte Address, Initial Access Latency (Dummy Cycles), Read Data
- Format 3.D: Command, 1-byte Address, Initial Access Latency (Dummy Cycles), Read Data
- Format 3.E: Command, 4-byte Address, Initial Access Latency (Dummy Cycles), Read Data
- Format 3.F: Command and Write Data
- Format 3.G: Command and 4-byte Address
- Format 3.H: Command, 1-byte Address, Write Data
- Format 3.I: Command, 4-byte Address, Write Data

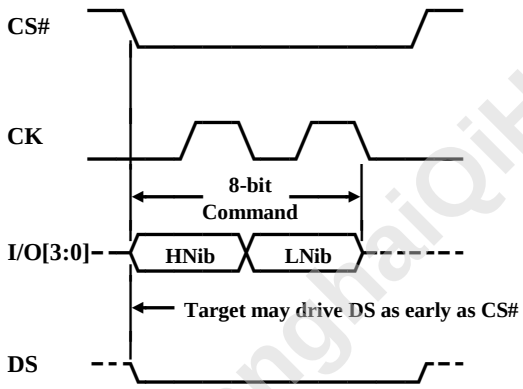


Figure 1 — Profile 1.0 4S-4D-4D Command Format 3.A, Command Only

5 Profile 1.0 4S-4D-4D Transaction Formats (cont'd)

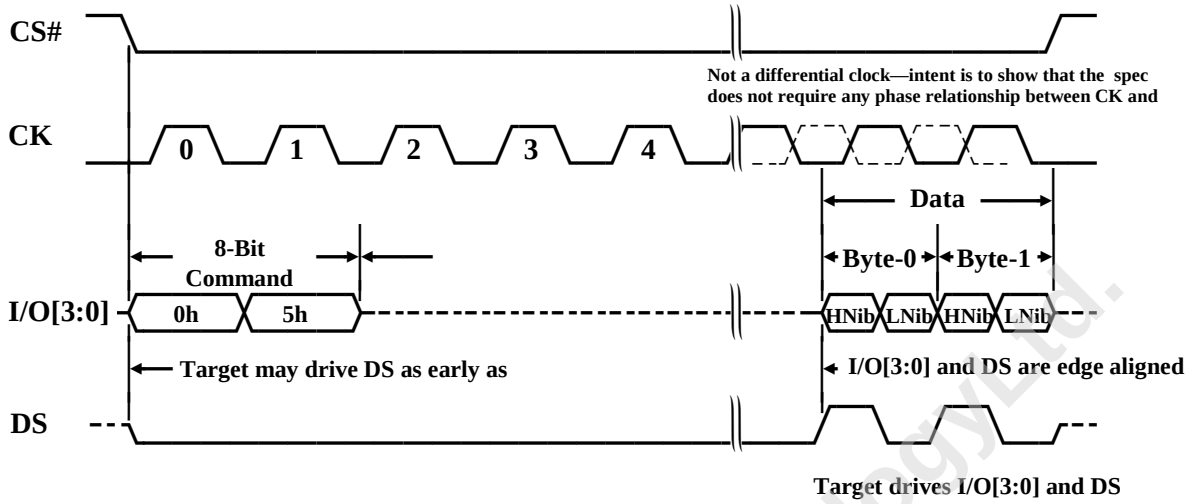


Figure 2 — Profile 1.0 4S-4D-4D Command Format 3.B, Read Status Register

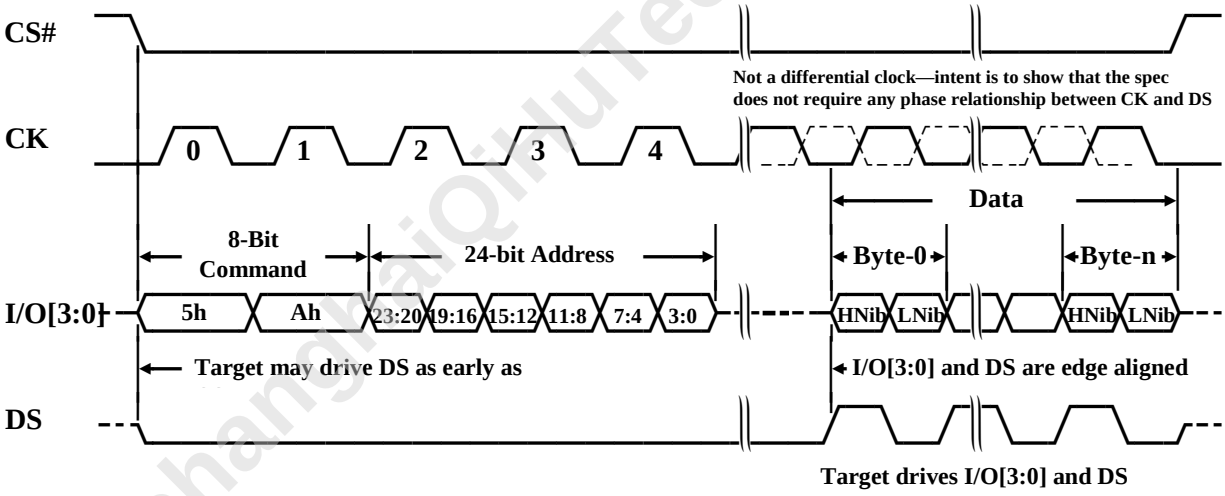


Figure 3 — Profile 1.0 4S-4D-4D Command Format 3.C, Read SFDP

5 Profile 1.0 4S-4D-4D Transaction Formats (cont'd)

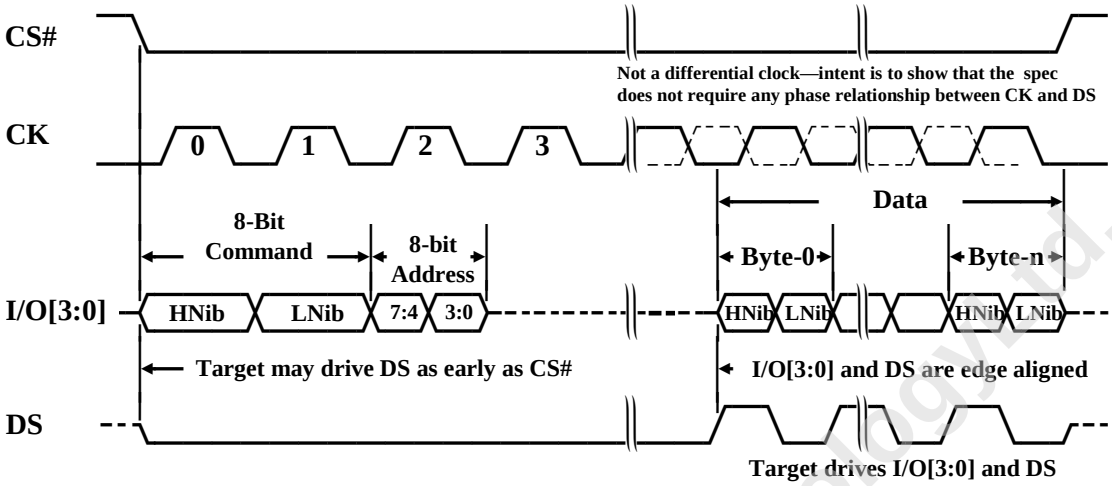


Figure 4 — Profile 1.0 4S-4D-4D Command Format 3.D, 1-Byte Address, Read 'n' bytes of Data

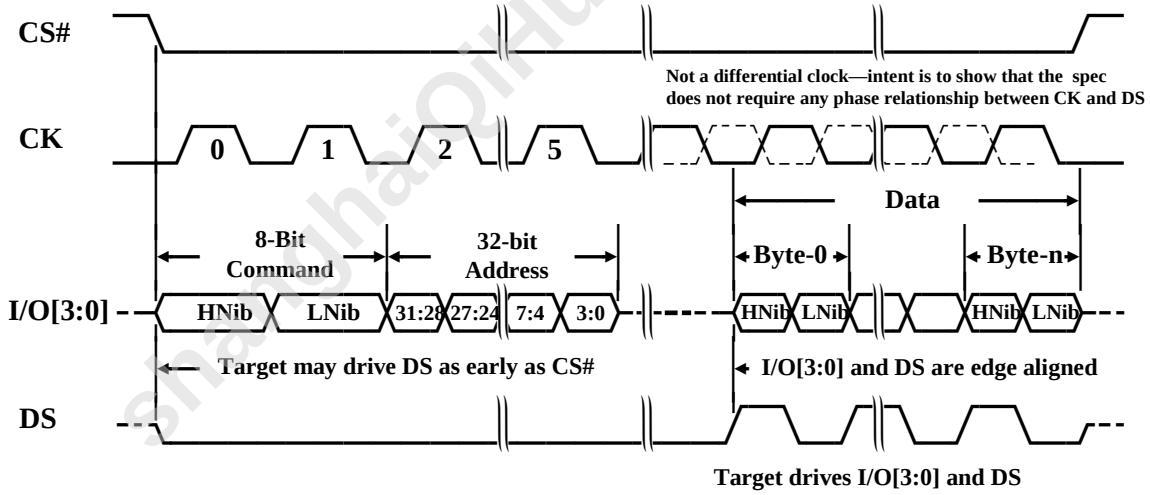


Figure 5 — Profile 1.0 4S-4D-4D Command Format 3.E, Fast Read 'n' Bytes of Data

5 Profile 1.0 4S-4D-4D Transaction Formats (cont'd)

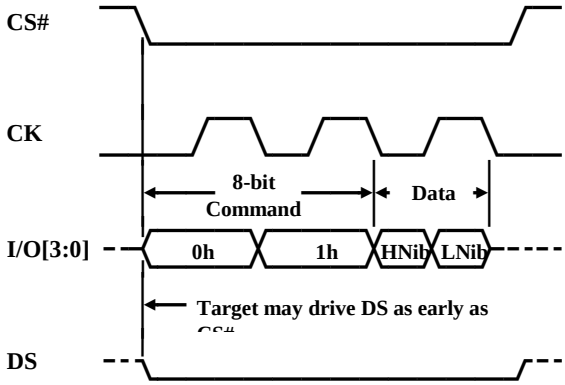


Figure 6 — Profile 1.0 4S-4D-4D Command Format 3.F, Write a Single Byte

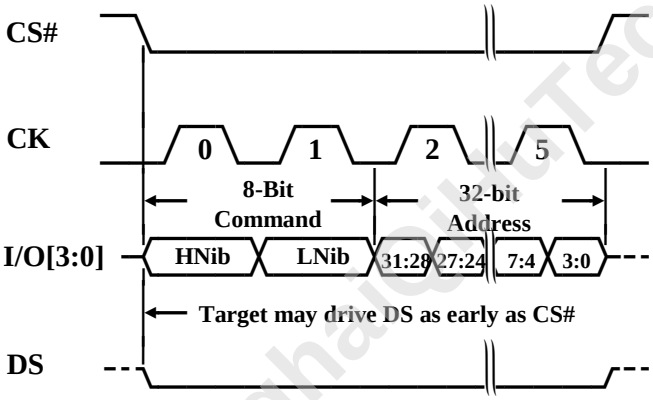


Figure 7 — Profile 1.0 4S-4D-4D Command Format 3.G, Command and 4-Byte Address

5 Profile 1.0 4S-4D-4D Transaction Formats (cont'd)

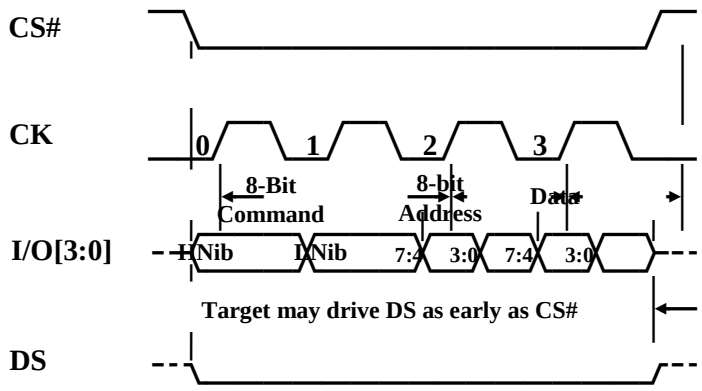


Figure 8 — Profile 1.0 4S-4D-4D Command Format 3.H, 1-Byte Address, Write 1-Byte Data

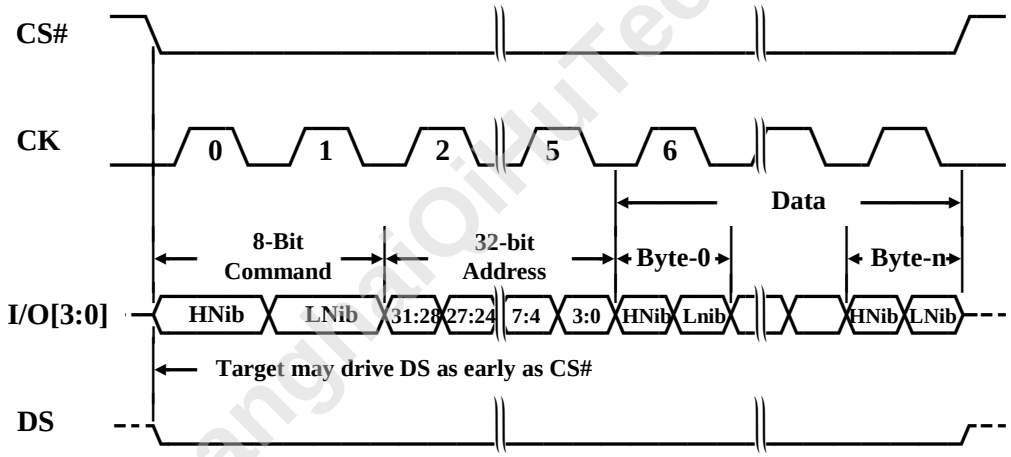


Figure 9 — Profile 1.0 4S-4D-4D Command Format 3.I, 4-Byte Address, Write 'n' Bytes of Data

6 Signal Assignments for 24-ball FBGA Footprint

The pin assignments of the x4 are identical to the x8 footprint with the exception that the I/O[7:4] signals are not used.

Table 4 — Signal Assignments for 24-ball FBGA Footprint

Ball Location	xSPI Signal
A1	No Ball
A2	RFU / RSTO#
A3	RFU / CS2#
A4	RFU / RESET#
A5	RFU / INT#
B1	RFU / CK#
B2	CK
B3	V_{SS}
B4	V_{DD}
B5	RFU
C1	V_{SS}IO
C2	CS#
C3	DS
C4	IO2
C5	RFU / VPP
D1	V_{DD}Q
D2	IO1
D3	IO0
D4	IO3
D5	IO4*
E1	IO7*
E2	IO6*
E3	IO5*
E4	V_{DD}Q
E5	V_{SS}Q

* IO4 to IO7 are used by Octal I/O devices, but are not used by Quad I/O devices.

Annex A (informative) Differences between revisions

This annex briefly describes the editorial changes to incorporate inclusive terminology to JESD251-1, published October 2018 as approved by the Serial Flash TG (JC424_3) to be published as JESD251-1.01.

Updated Table of Contents to include this Annex A

Globally changed

1) Non-inclusive word to “initiator”
2) Non-inclusive e word to “Target”
3) Non-inclusive word to “target”

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